

# Compal Confidential

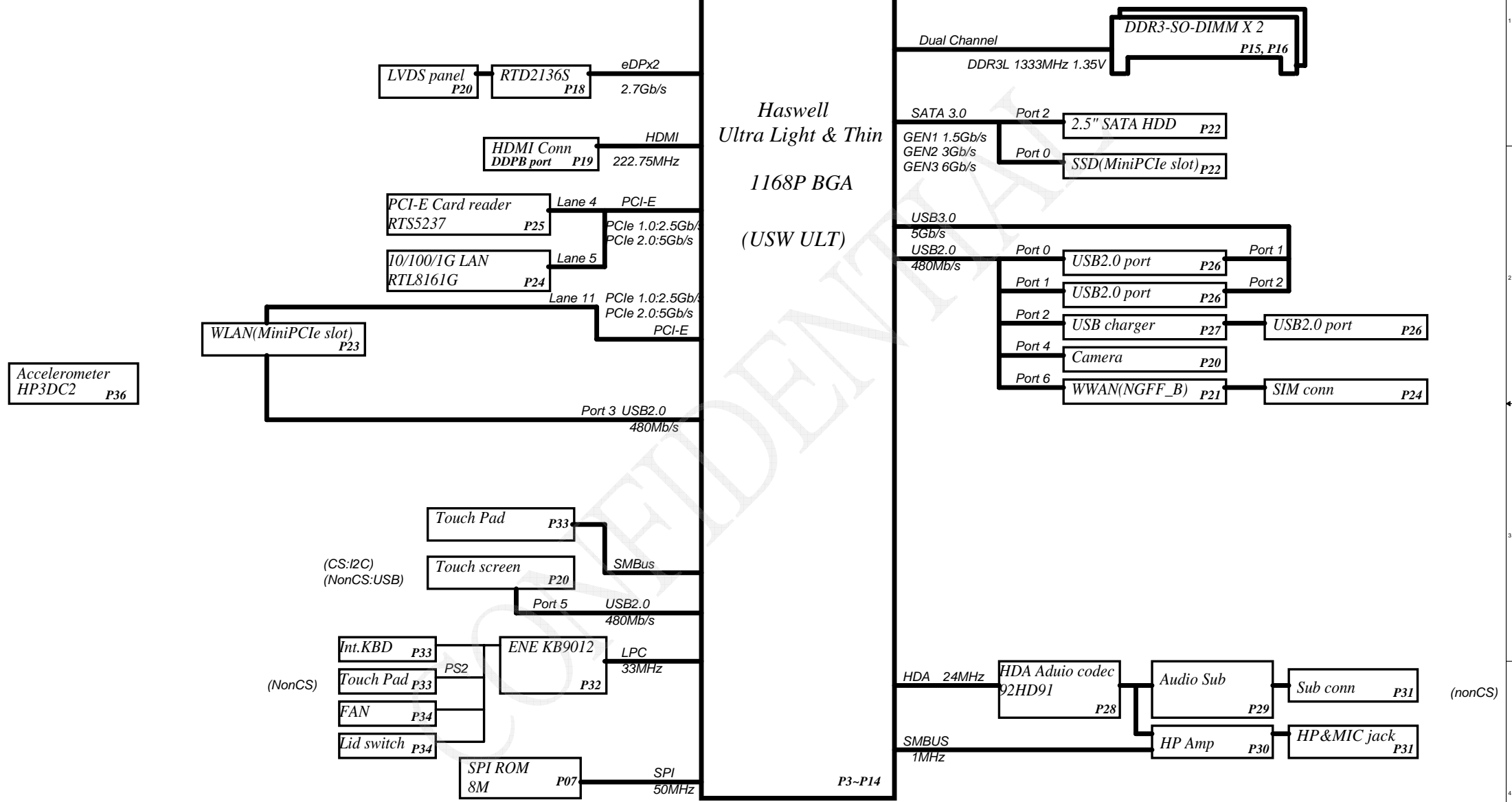
## Hasswell M/B Schematics Document

Intel ULV Processor with LPDDR3/DDR3L

Date : 2013/04/10

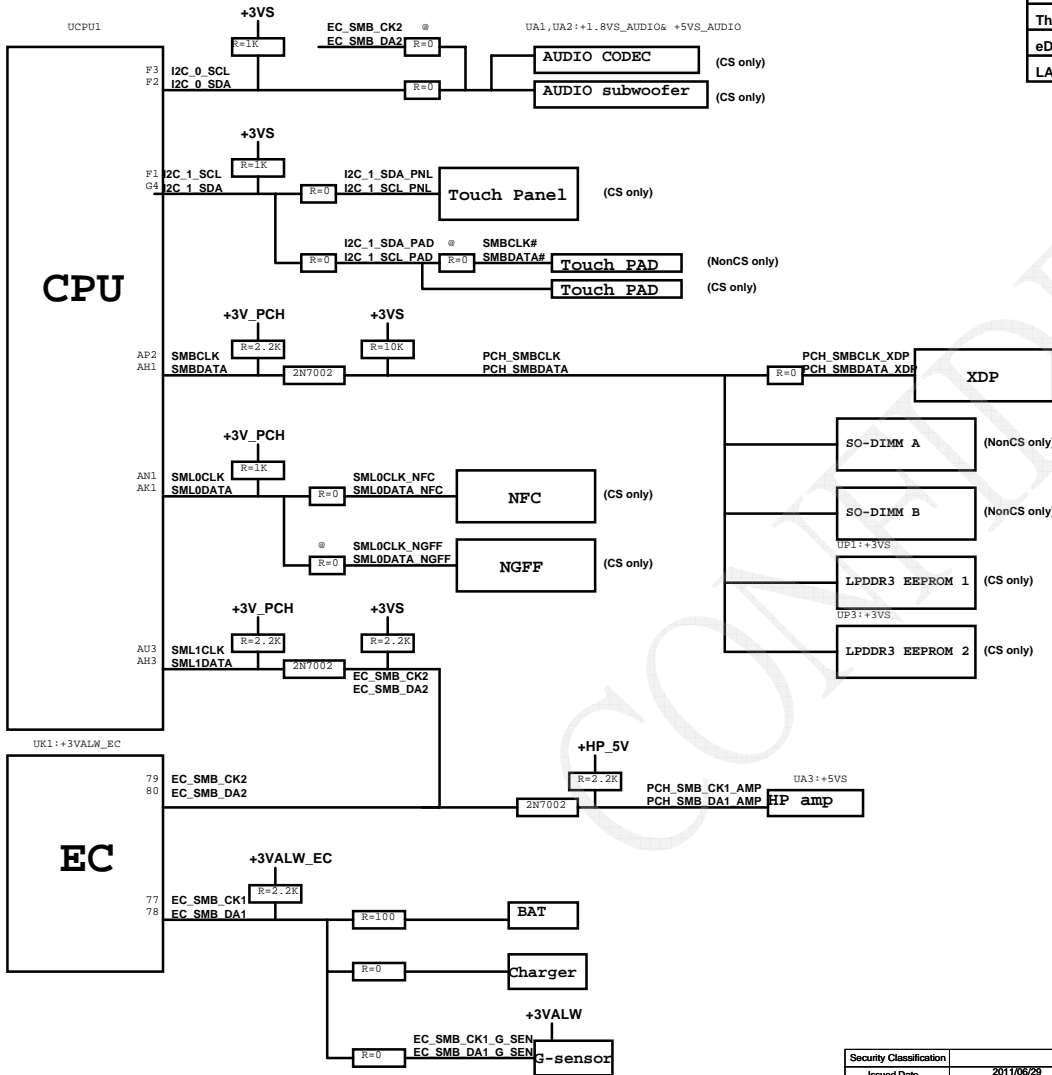
Version 1.0

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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.05V	SUSP#	
+1.8V	SYSON	PM_SLP_S5# / PM_SLP_S4#
+1.2V_1.35V	SYSON	PM_SLP_S5# / PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.8VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+1.05VS_MODPHY	X	MPHY_PWREN
+0.6V_0.675VS	X	SM_PG_CTRL
+VCC_CORE	X	VR12.5_VR_ON

@ is NO SMT part (empty)



### <Power gating GPIO,wake ,INT and RST>

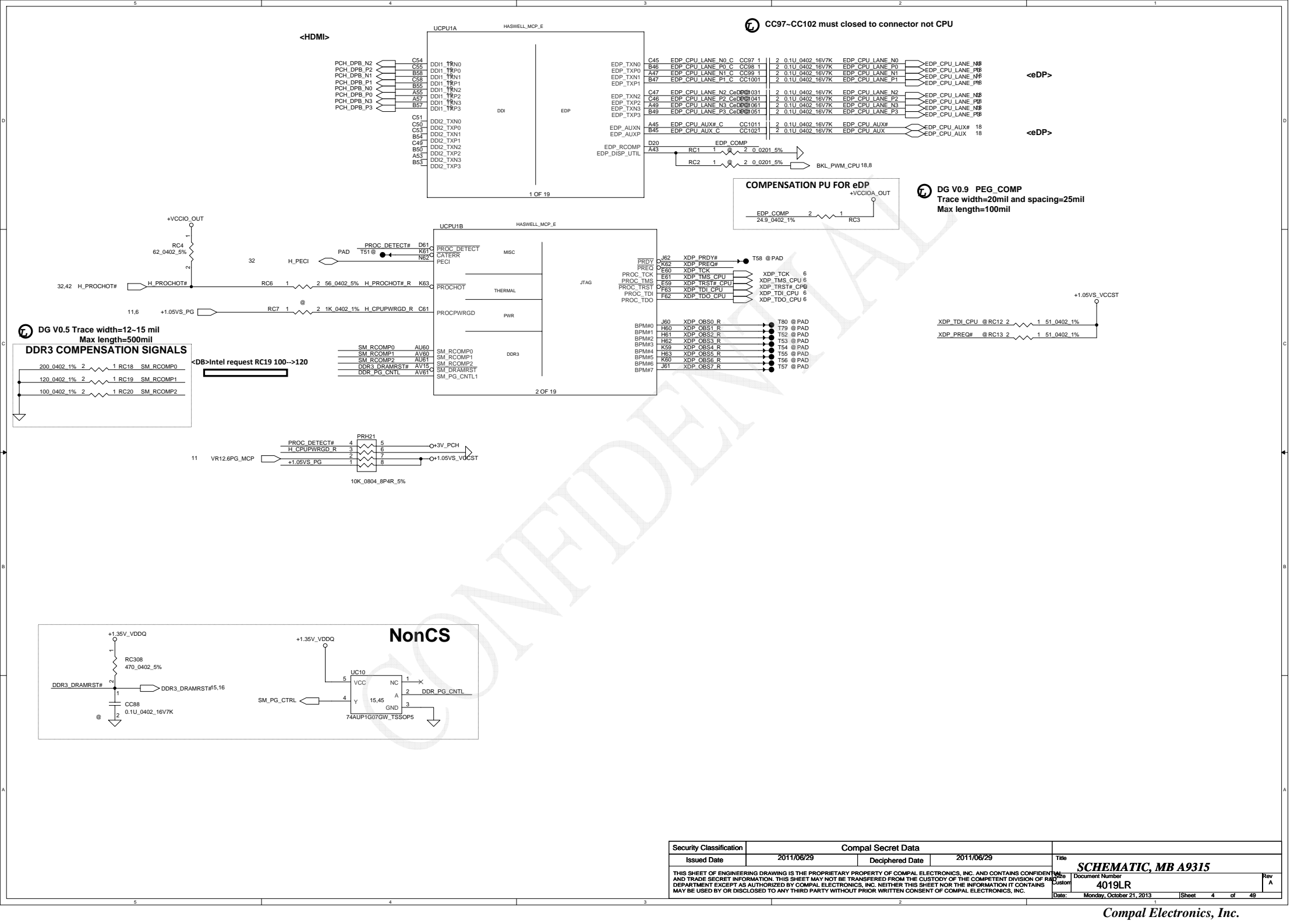
Device	Power gating GPIO	Enable (ON) CPU IC HW part	RST/RQ	Wake/INT
NGFF SSD	X(Not support)			
NGFF WWAN	X(Not support)			
NGFF WLAN/BT WLAN (MiniPCle) *	GPIO83	H H Load switch	GPIO34 *	GPIO54 *
USB3.0 CONN	GPIO13	L L USB switch		
USB3.0 CONN(Charger)	GPIO43	H H USB charger		
Card reader (PCI-E)	GPIO60	H H Load switch	GPIO93	GPIO94
USB2.0 Camera	GPIO25	H H Load switch		
Touch Panel	GPIO89	H H Load switch	GPIO52	GPIO50
Touch Pad -NonCS Touch Pad -CS *	GPIO88	L L PMOS		GPIO55 *
WWAN	GPIO84	H H Load switch		
SATA HDD/SSD	GPIO90	H H Load switch	GPIO38 X(Not support)	
mSATA	GPIO86	H H Load switch	DEVSLP2#/GPIO39	
Audio DSP + codec	GPIO76	H H Load switch	X(Not support)	
Thermal (EC)	X(Not support)			
eDP*	V	Load switch		
LAN (PCI-E)	GPIO12	H L Load switch	GPIO91	GPIO92

### <USB2.0 port>

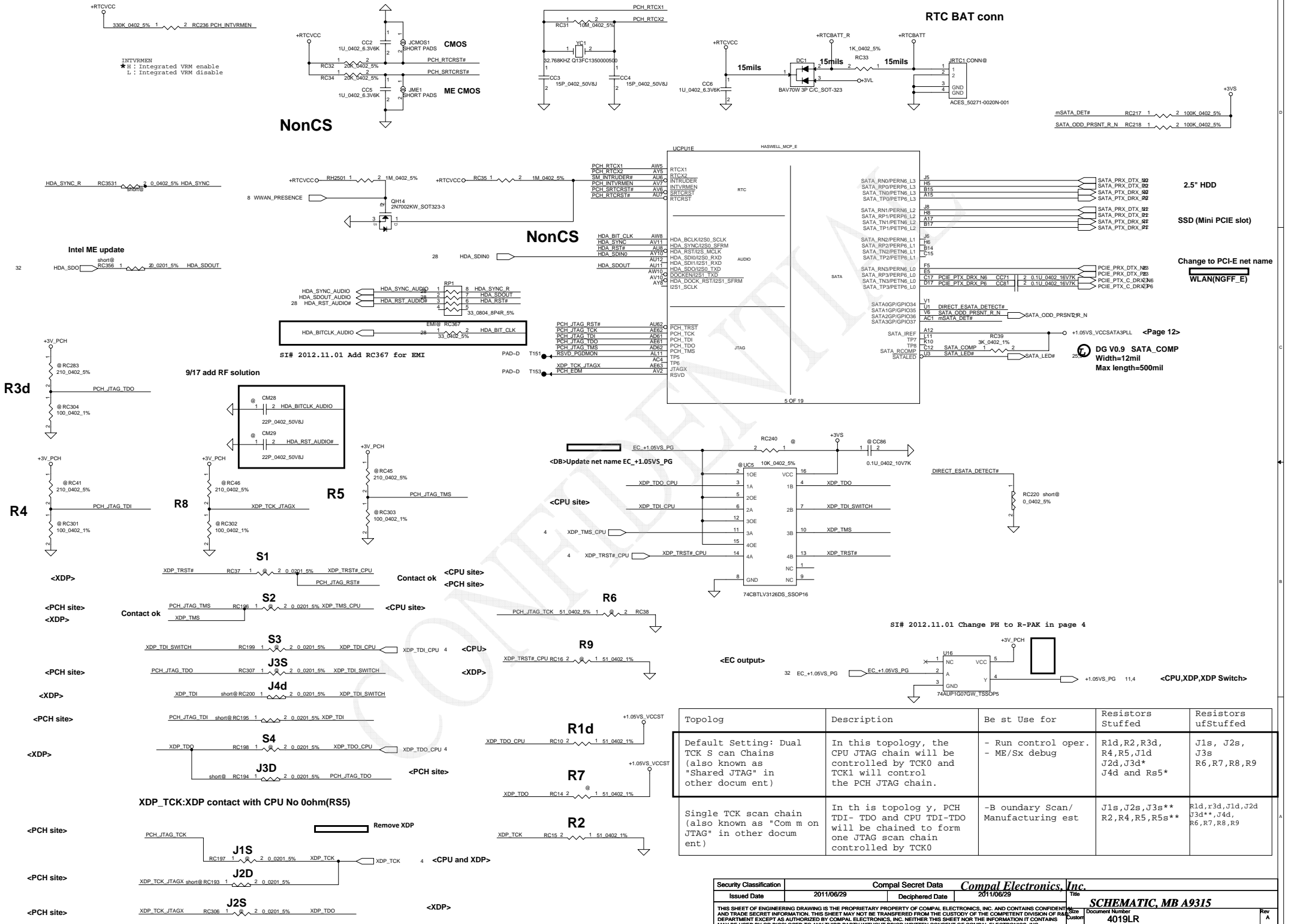
USB2.0 port	DESTINATION	
	CS	NonCS
0	USB 2.0(left side)	USB 2.0(left side)
1	USB 2.0(left side)	USB 2.0(left side)
2	USB 2.0(right side)	USB 2.0(right side)
3	WLAN (NGFF)	WLAN (MiniPCle)
4	Camera	Camera
5	No contact	Touch screen
6	WWAN	WWAN
7	Finger printer	Finger printer

### <PCI-E,SATA,USB3.0>

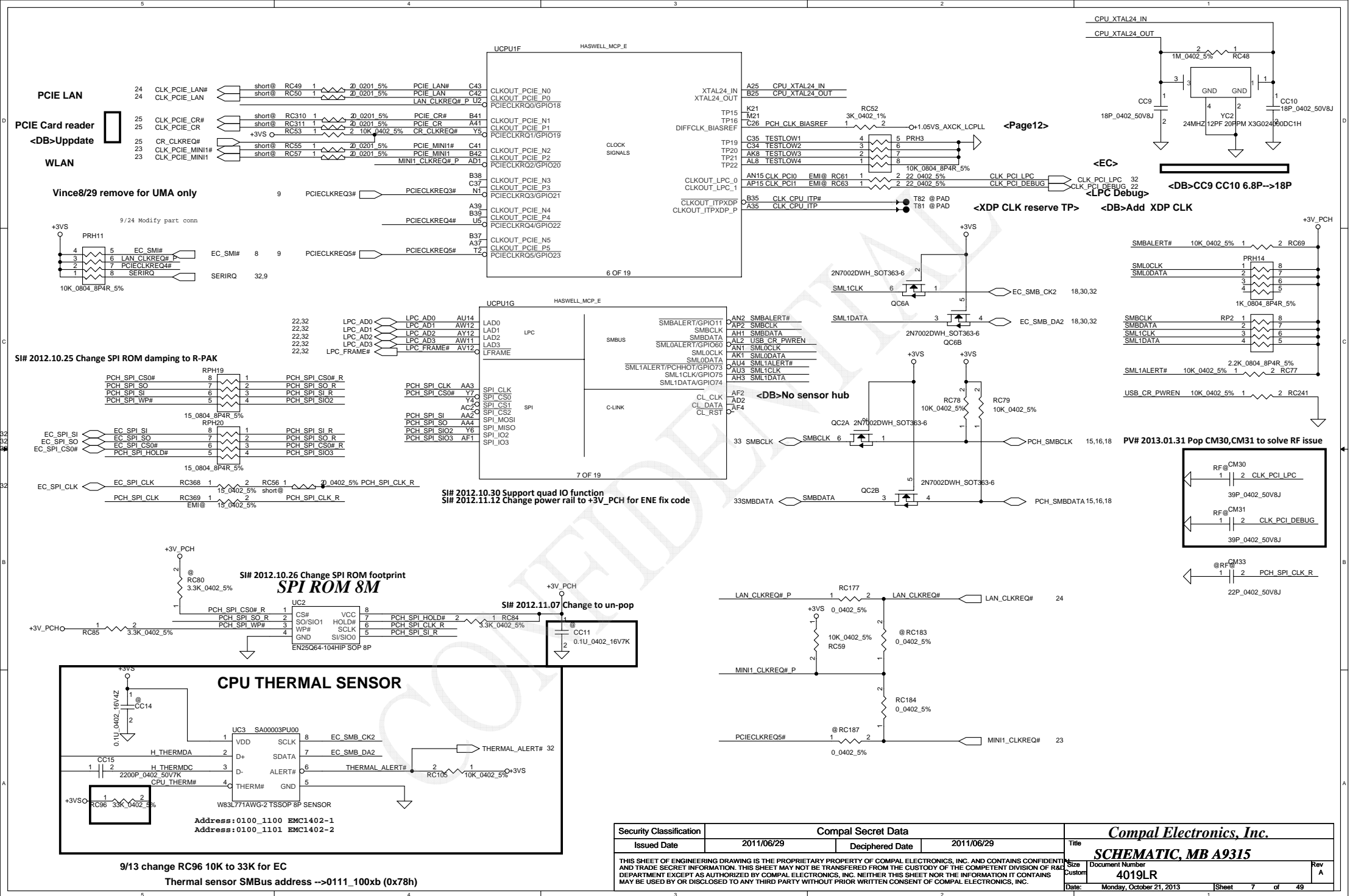
Lane#	PCI-E	SATA	USB3.0	DESTINATION	
				CS	NonCS
1			1	USB3.0	USB3.0
2			2	USB3.0	USB3.0
3	1		3	X(Not support)	X(Not support)
4	2		4	Card reader(PCI-E)	Card reader(PCI-E)
5	3			10/100/1000 LAN	10/100/1000 LAN
6	4				
7					
8					
9					
10					
11		3		WLAN (NGFF)	WLAN (MiniPCle)
12		2			
13		1		2.5"HDD	2.5"HDD
14		0		SSD(mSATA)	SSD(mSATA)







Topolog	Description	Be st Use for	Resistors Stuffed	Resistors uStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topology, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d***,J4d, R6,R7,R8,R9



PV# 2013.01.07 Add test point

DSWODVREN - On Die DSW VR Enable

★ H : Enable  
L : Disable

DSWODVREN RC254 2 1 330K 0402 5%  
DSWODVREN RC255 2 1 330K 0402 5%

Non Deep S3 RC91-->SMT  
Deep S3 RC93-->SMT

PV# 2013.01.30 Let AOAC\_PME# connect with WAKE# to support DS3 wake.

SI# 2012.10.25 Change RC106 to 10K

PANEL\_BKEN\_CPU PD 100K on Page20

<HDMI>

<HDMI>

<eDP HPD>

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9/12 reserve EC\_FB\_CLAMP\_TGL\_REQ# on GPIO16  
9/12 reserve DGPU\_GC6\_EN on GPIO17

9/13 remove EC\_FB\_CLAMP\_TGL\_REQ# for UMA only

9/12 reserve DGPU\_HOLD\_RST# on GPIO58

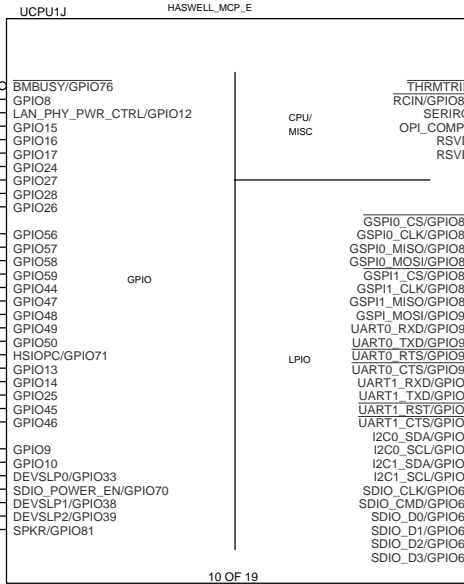
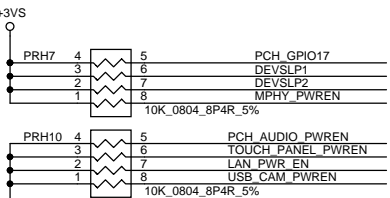
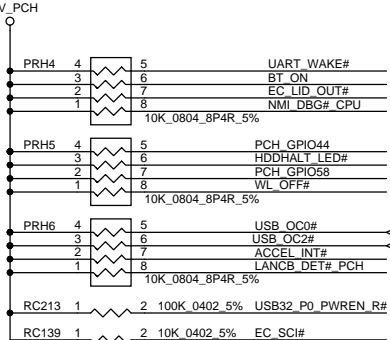
No sensor hub  
No sensor hub

No sensor hub

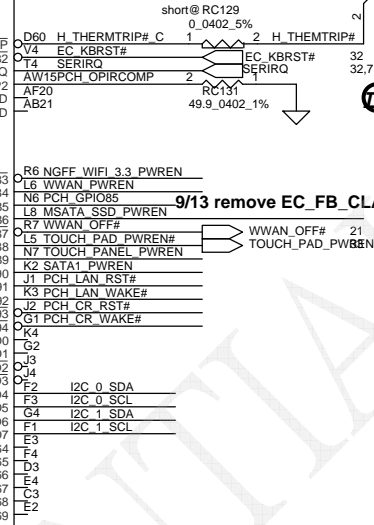
<DB>CS only PCH\_HP\_DET#

PCH\_GPIO81(HDA\_SPKR):NonCS only

SI# 2012.10.25 Change ACCEL\_INT#(PCH\_GPIO80) to GPIO46



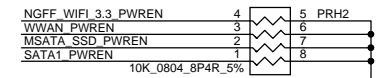
DG V0.9 PCH\_OPIRCOMP  
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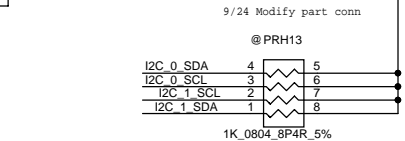
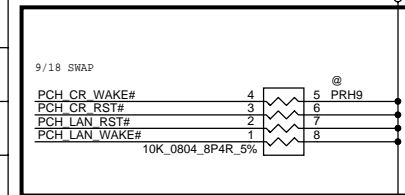
9/13 remove EC\_FB\_CLAMP\_TGL\_REQ# for UMA only

Boot BIOS Strap

PCH_GPIO86	Boot BIOS Location
0	SPI



	GPIO47 LPDDR3_ID1	GPIO48 LPDDR3_ID2	GPIO49 LPDDR3_ID3
Hynix 8G/1600 H9CCNNN8JTMLAR	0	0	0
Samsung 8G/1600 K4E8E304EB-EGCE	0	0	1
Elpida 8G/1600 EDF8132A1MC-GD-F	0	1	0



SI# 2012.11.07 Change RC360,PRH9,RC290 to un-pop

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10/100/1G LAN

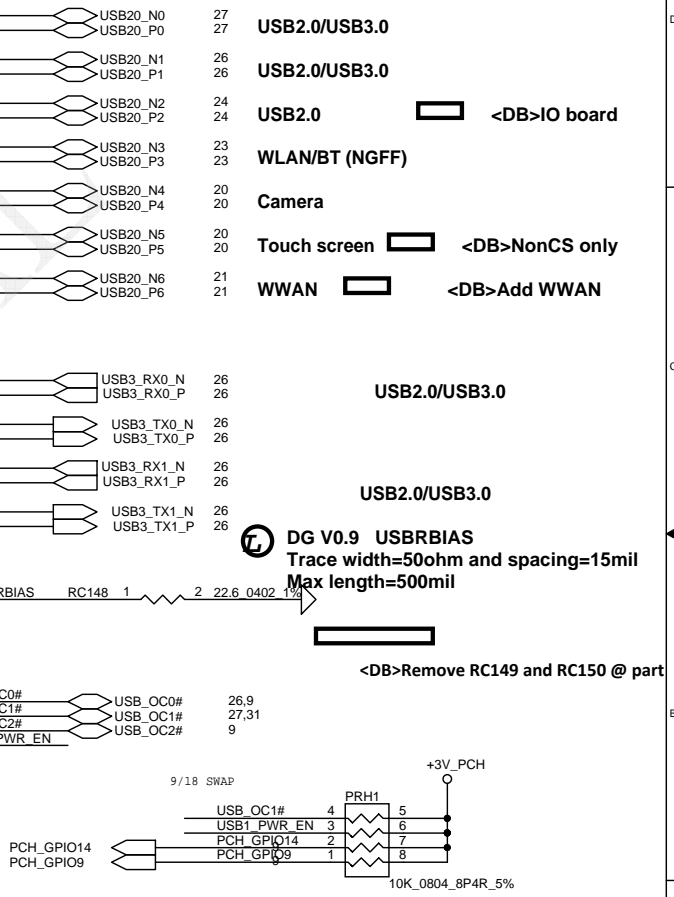
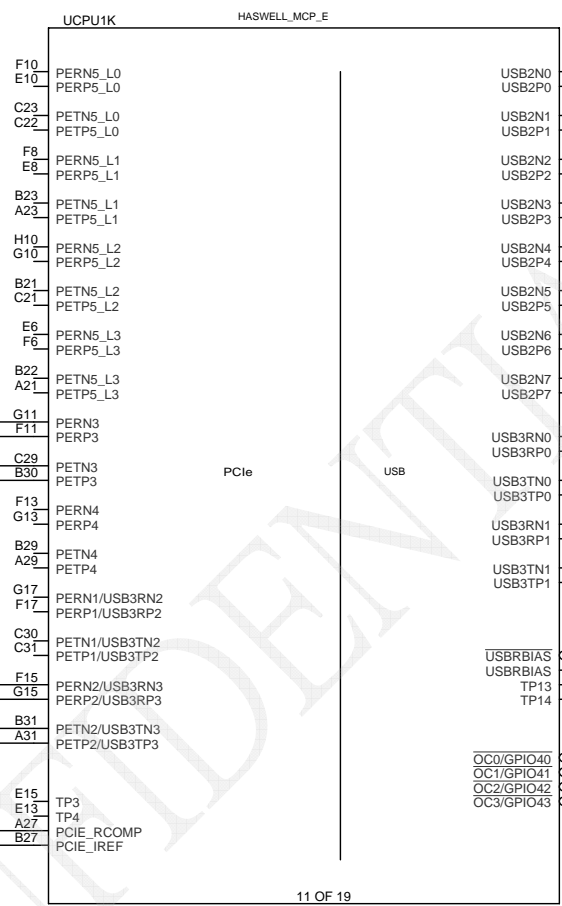
PCI-E Card reader

Vince8/29 remove for UMA only

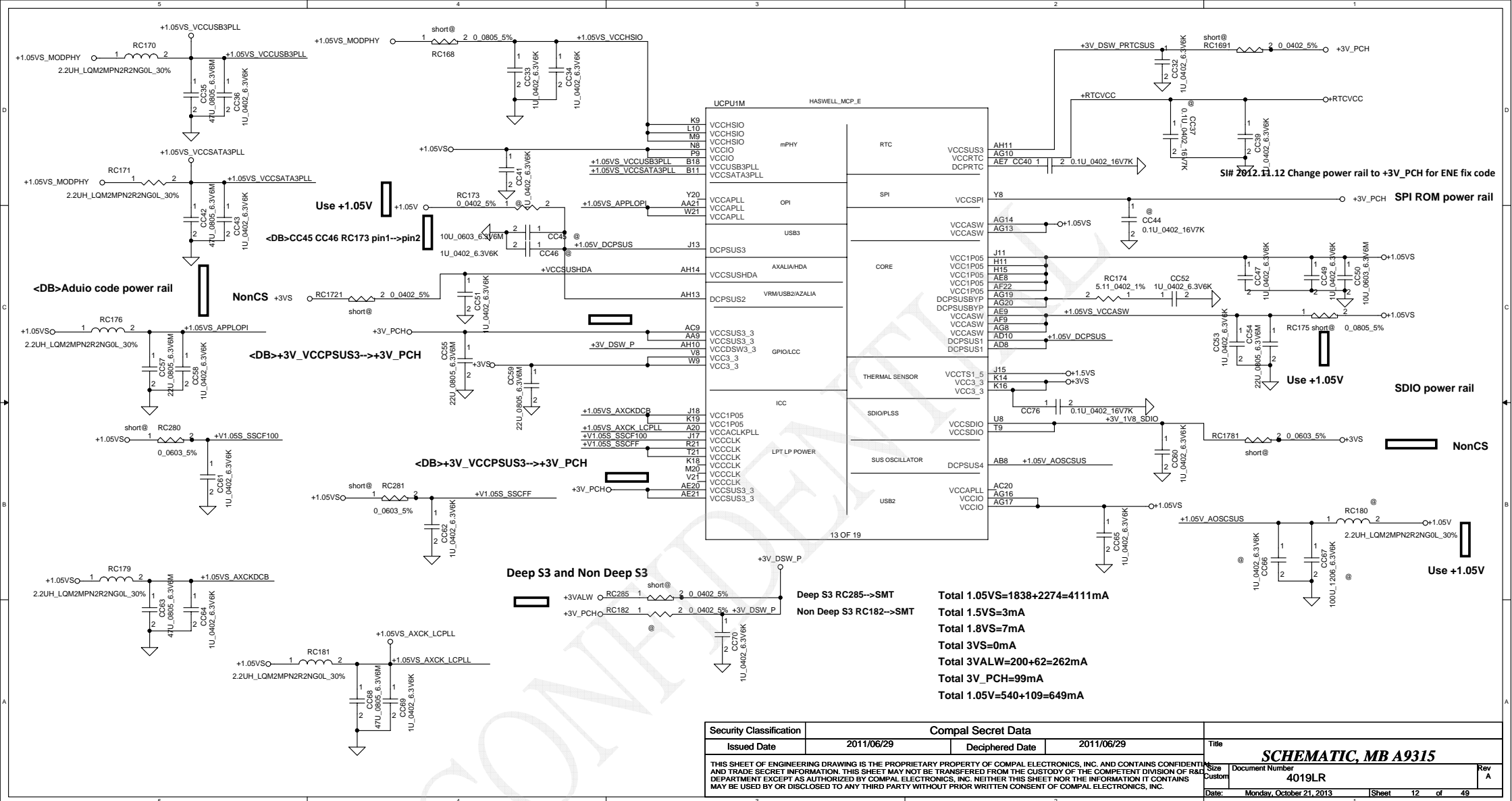
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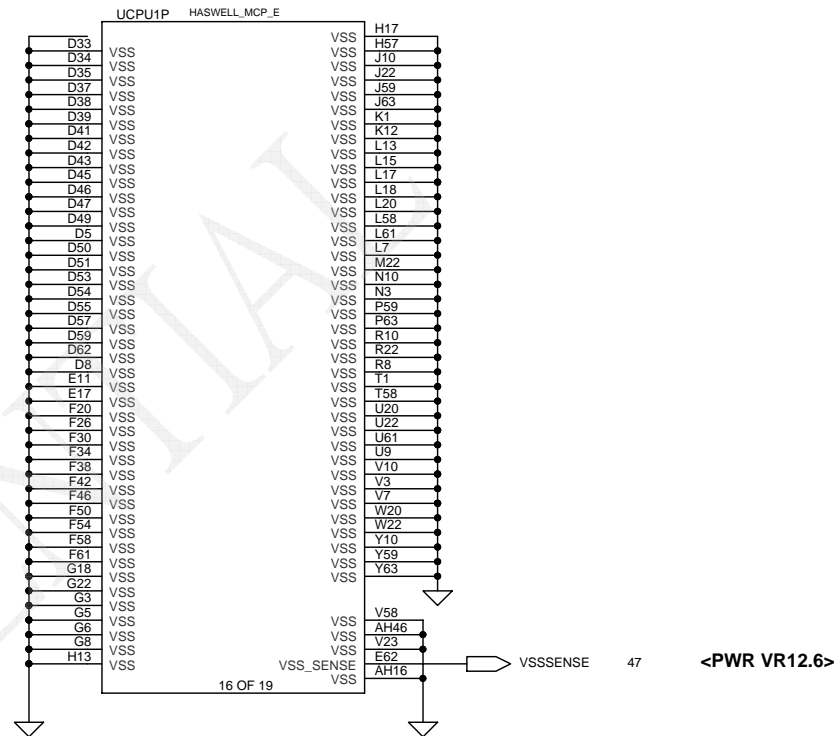
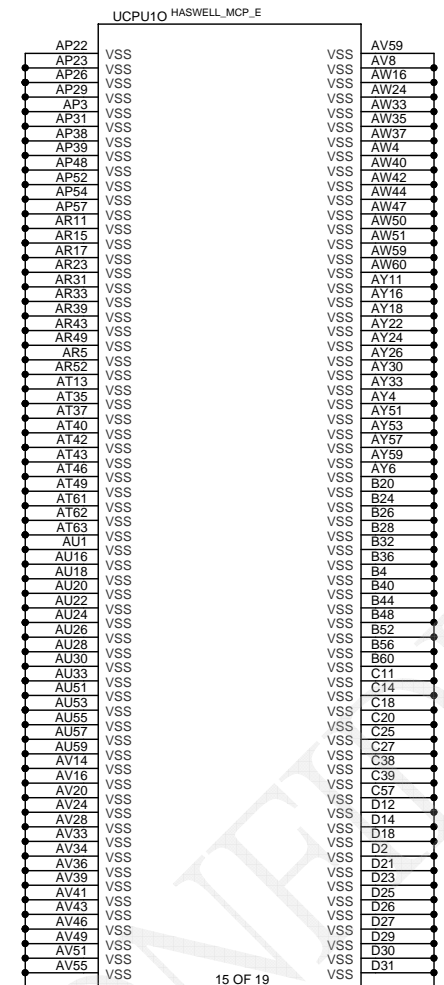
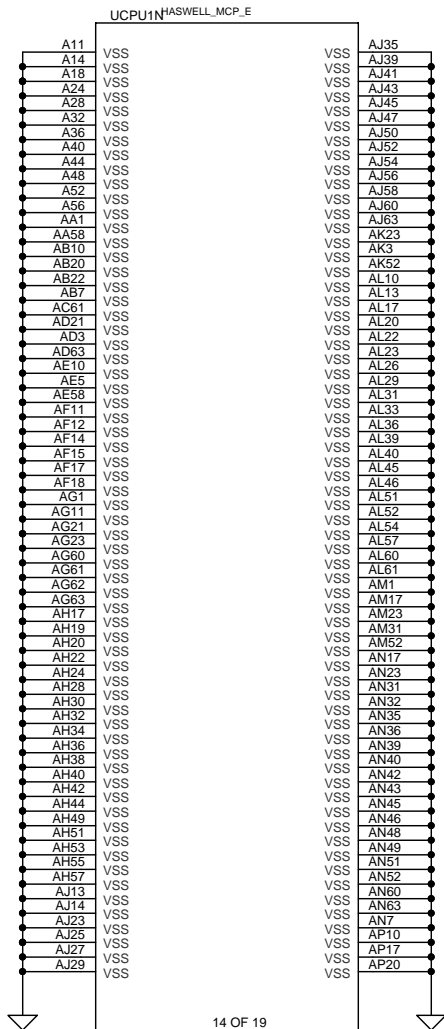
DG V0.9 PCIE\_RCOMP  
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Max length=500mil

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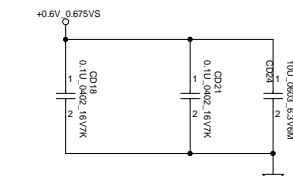
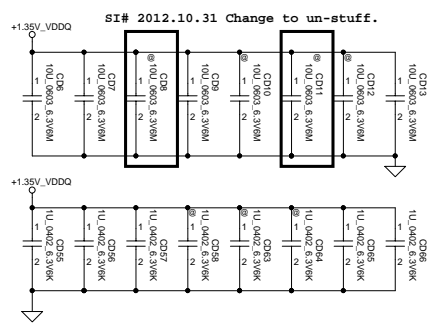
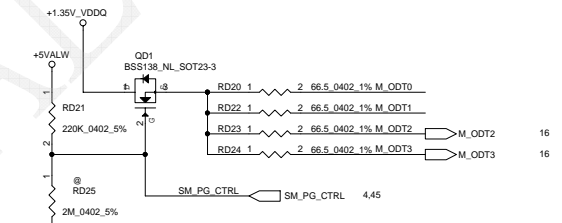
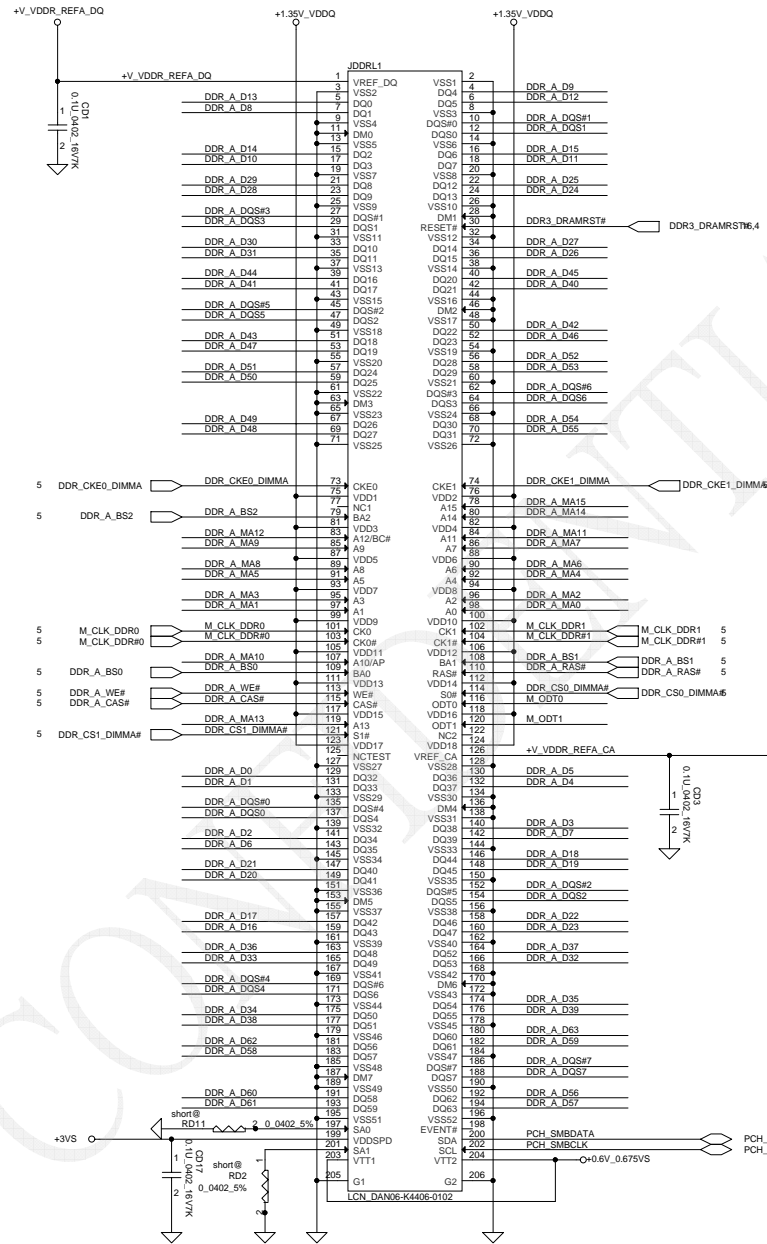
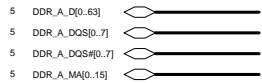






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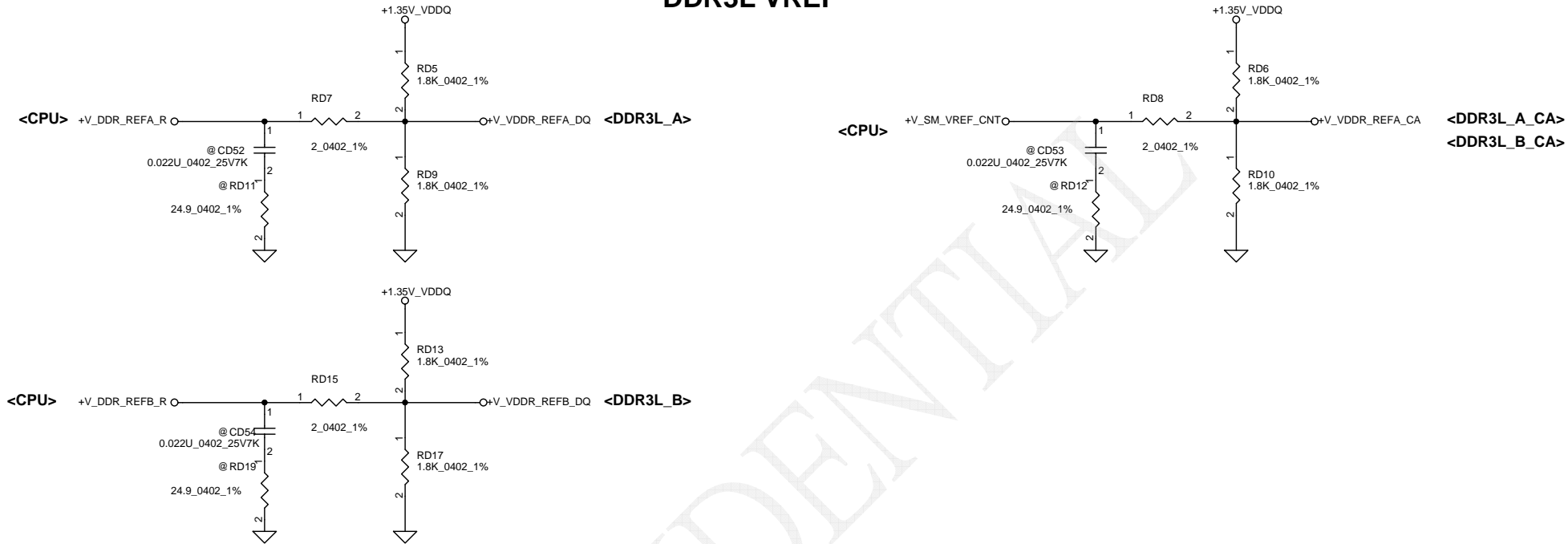


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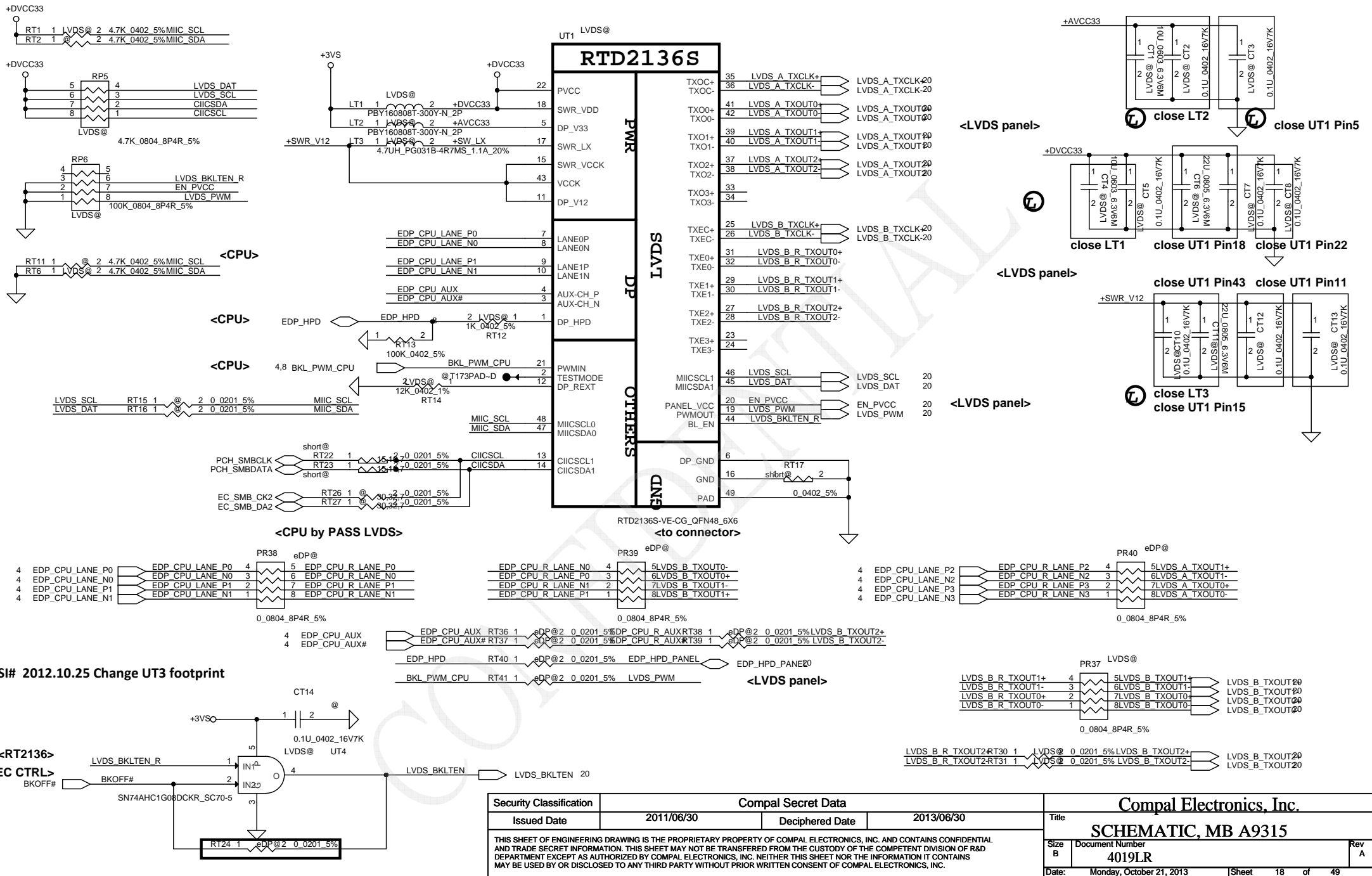


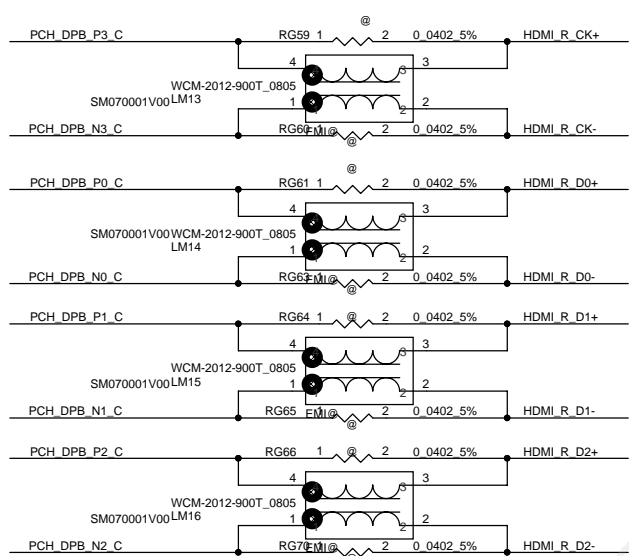
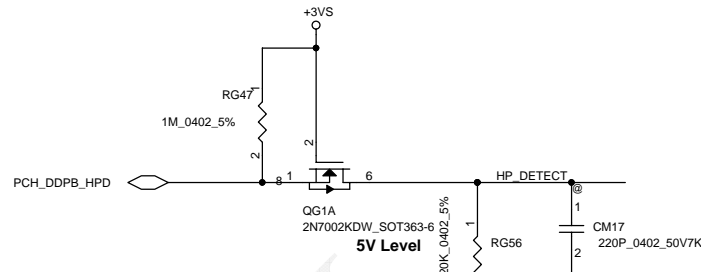
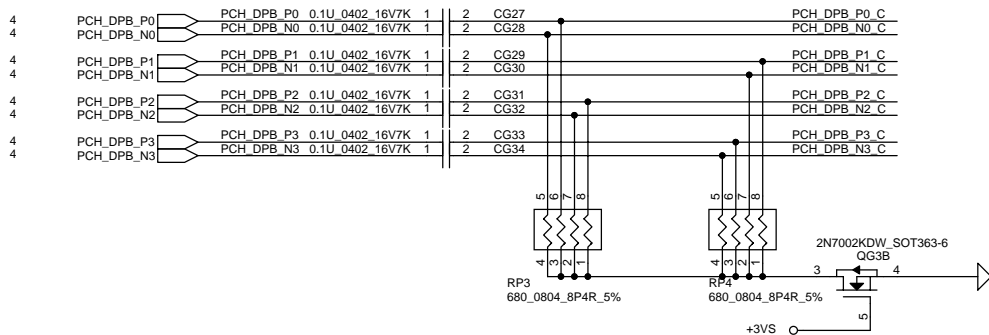


DDR3L VREF

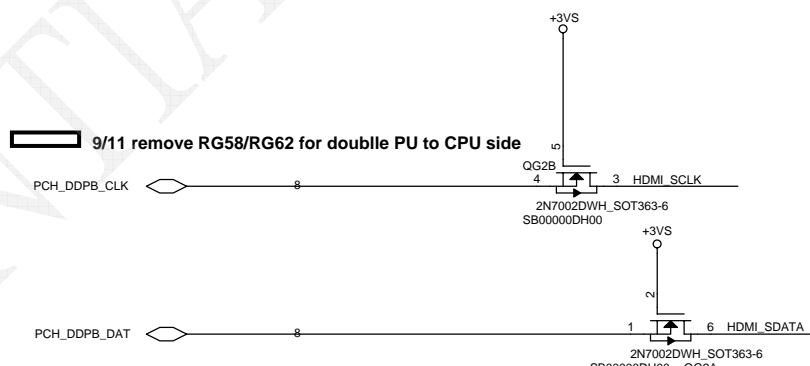


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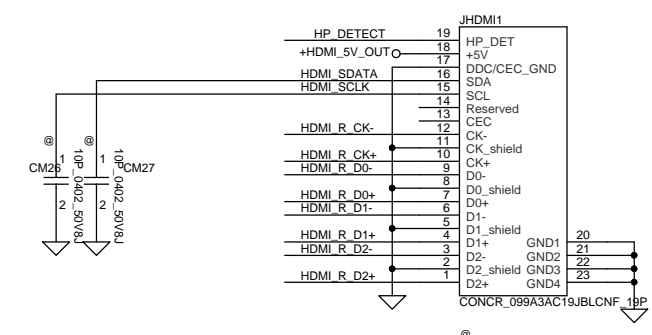
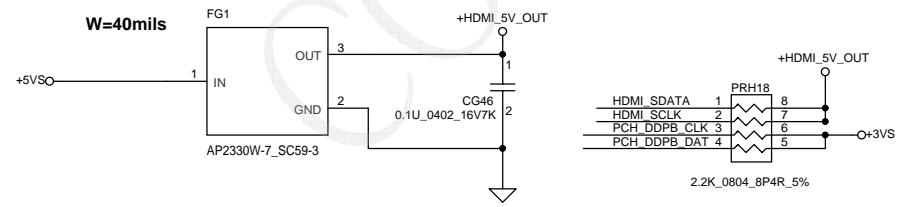


9/11 remove RG58/RG62 for double PU to CPU side

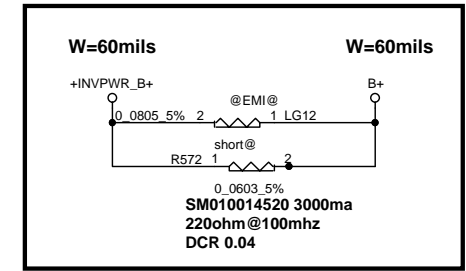
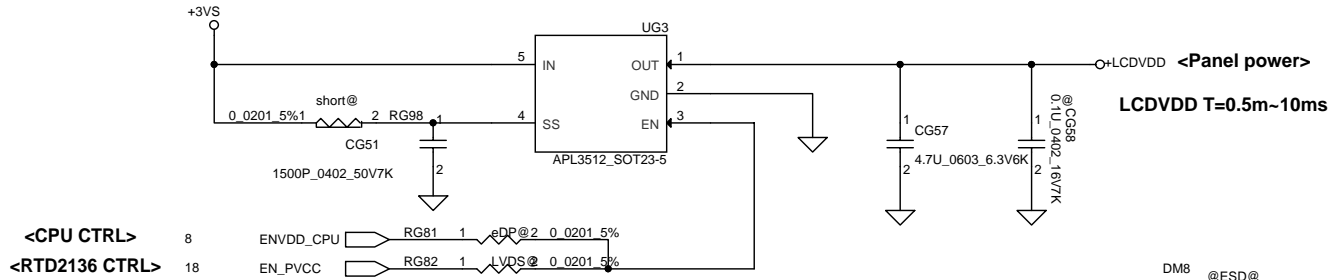


5V PULL UP IN CONNECTER SIDE

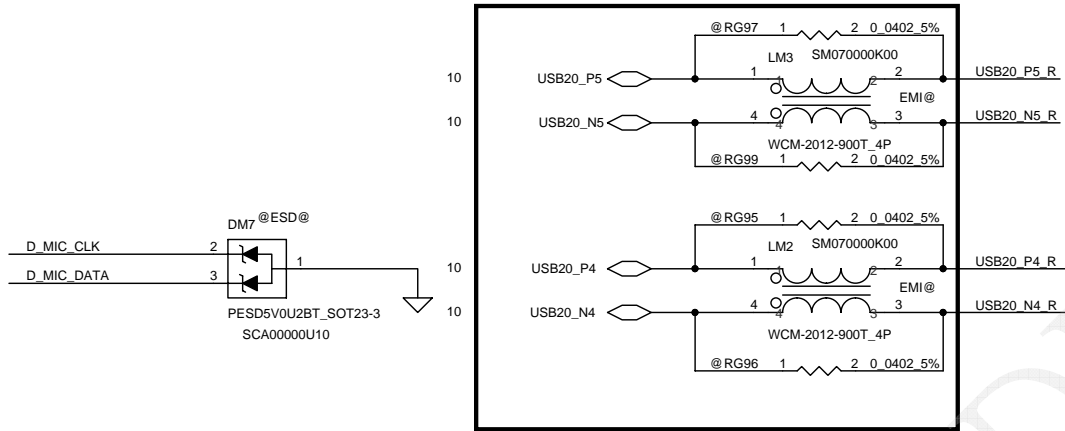
HDMI Conn.



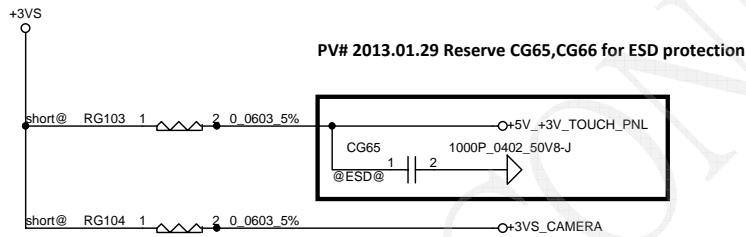
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PV# 2013.01.24 Add R572 to support FHD black light current.

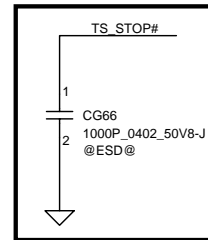


SI# 2012.10.25 Add RG103 short pad for touch panel and RG104 for CAMERA, and reserve UG4, CG53, CG54

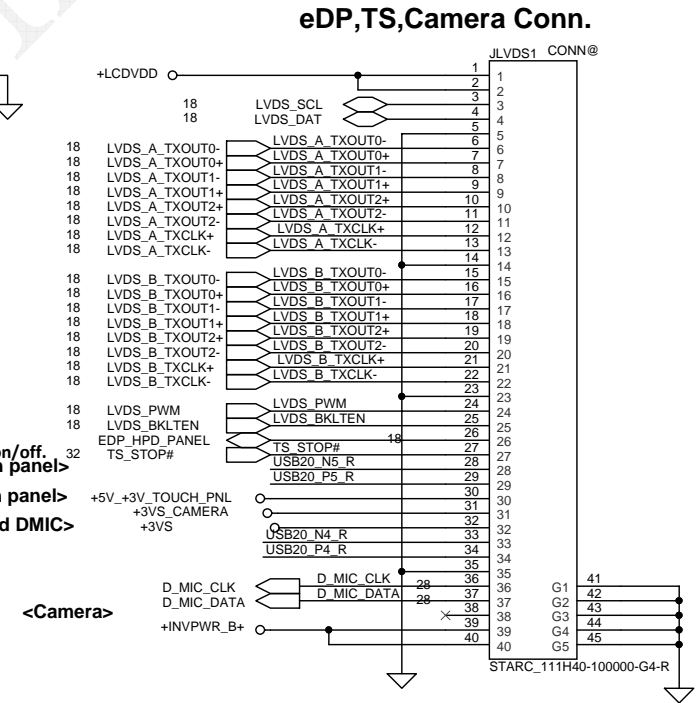


PV# 2013.01.29 Reserve CG65,CG66 for ESD protection

SI# 2012.10.25 Add TS\_STOP# to control touch screen power on/off.

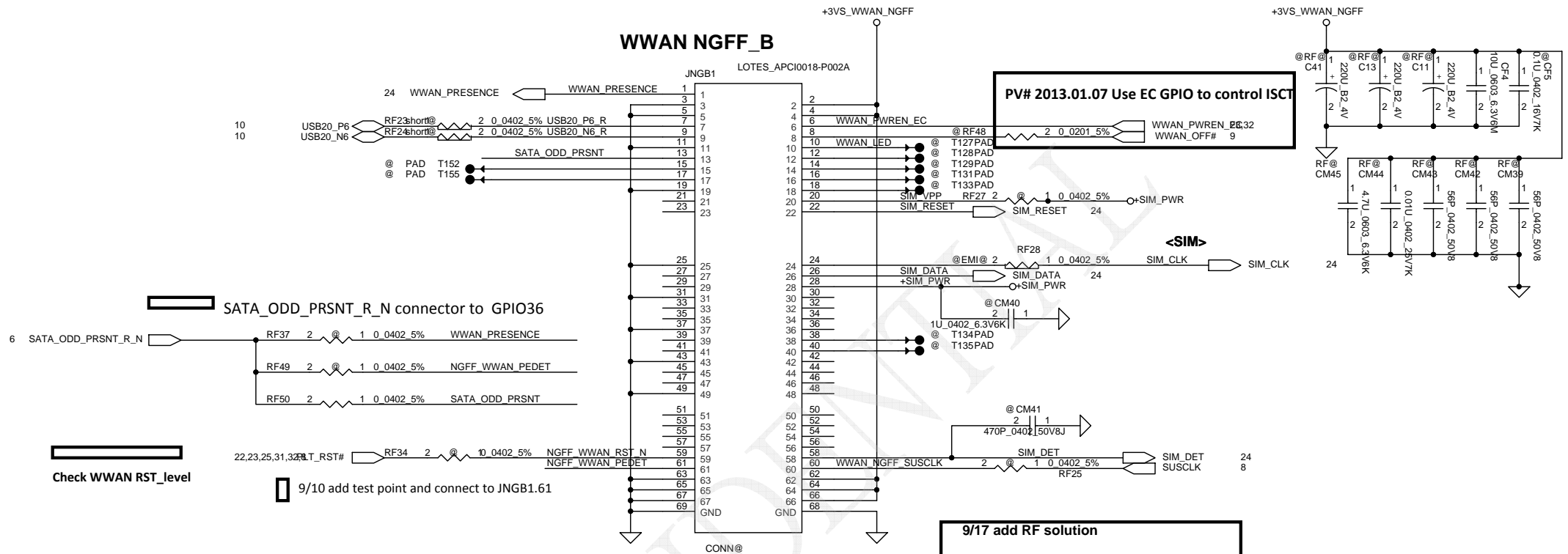


**<USB Touch panel>**  
**<Touch panel>**  
**<Camera and DMIC>**

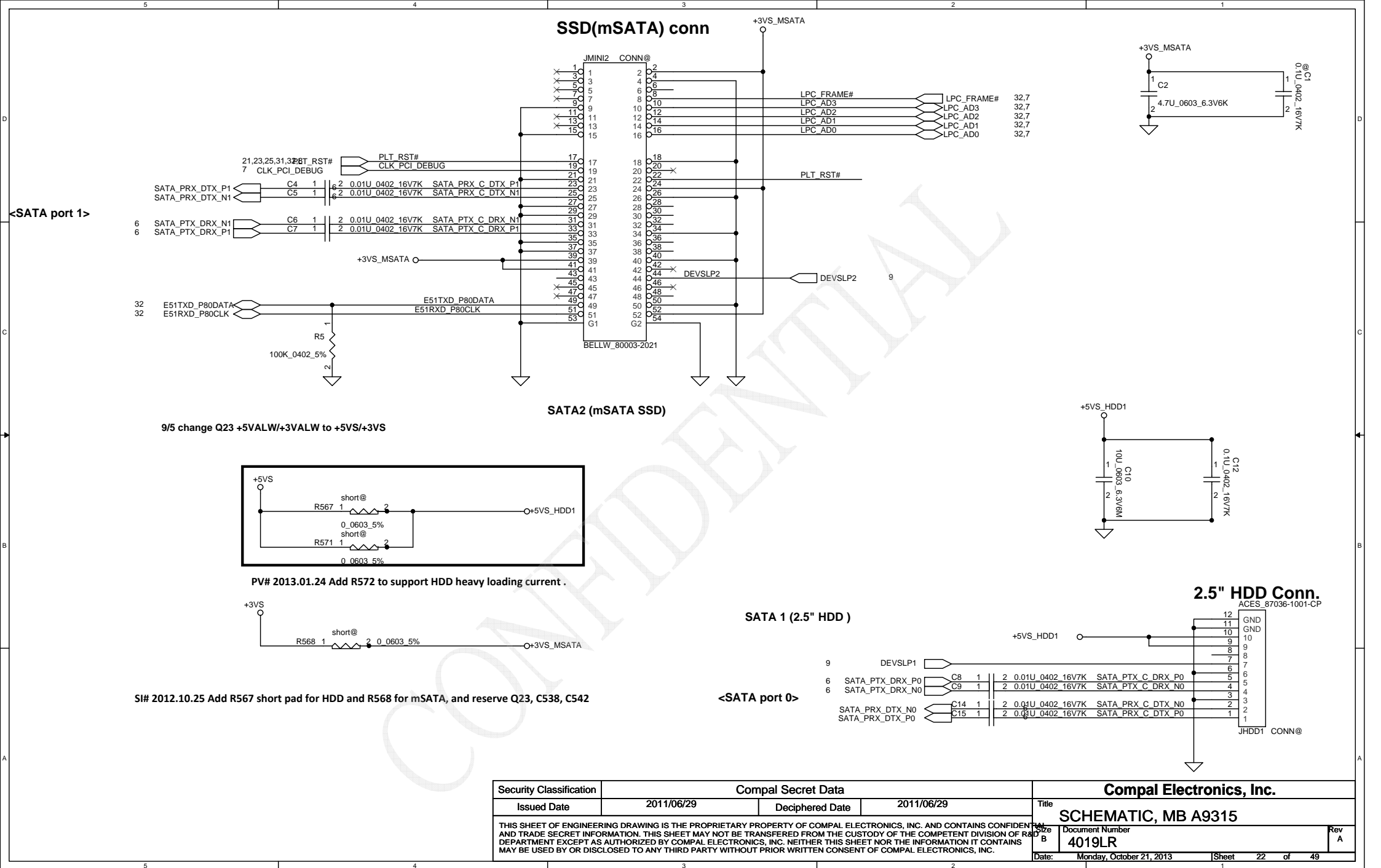


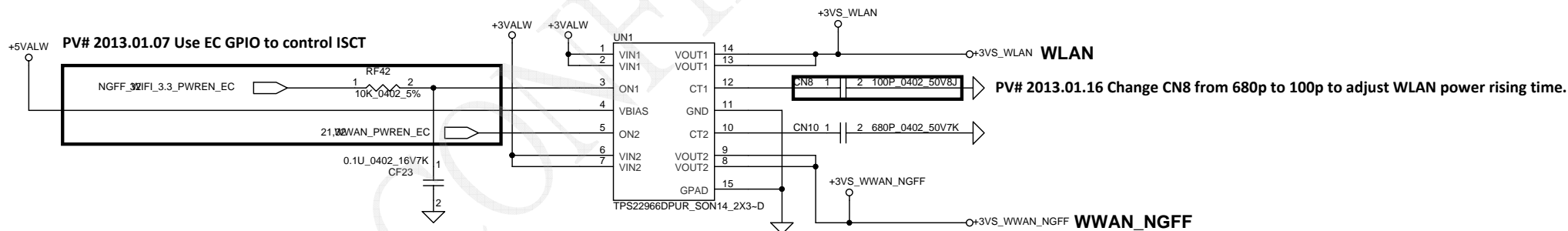
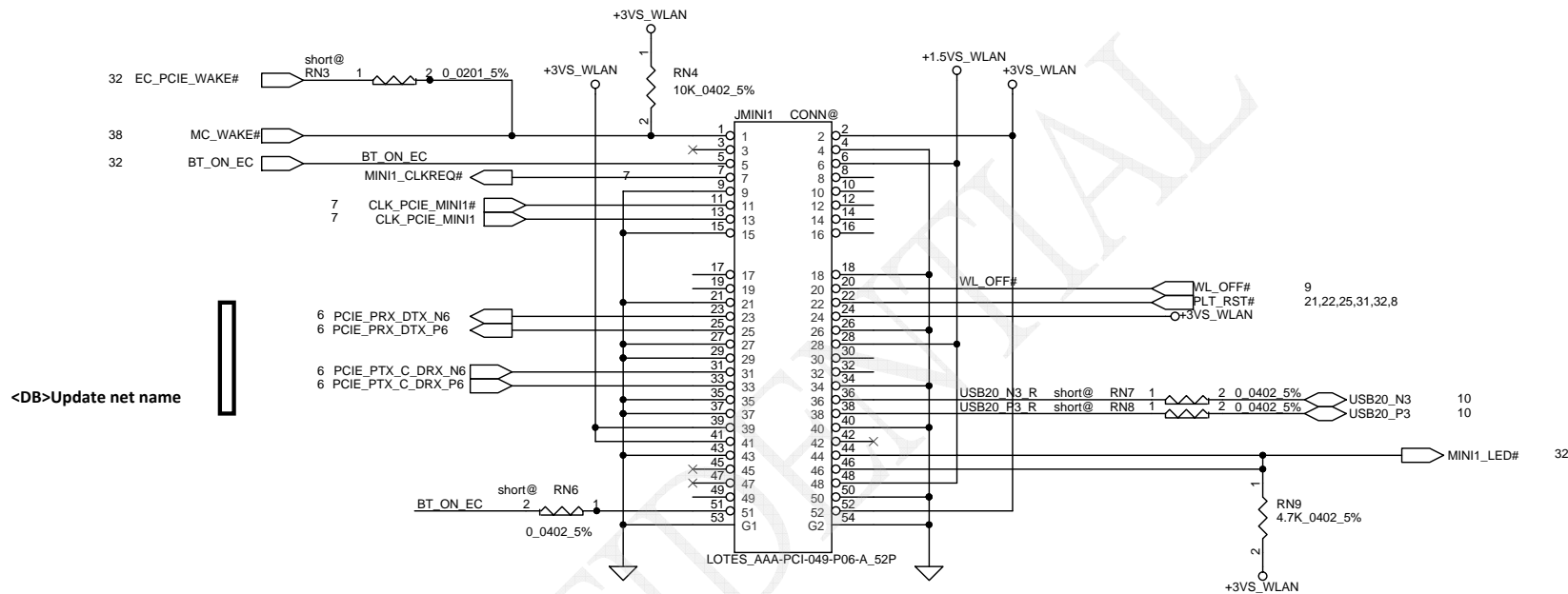
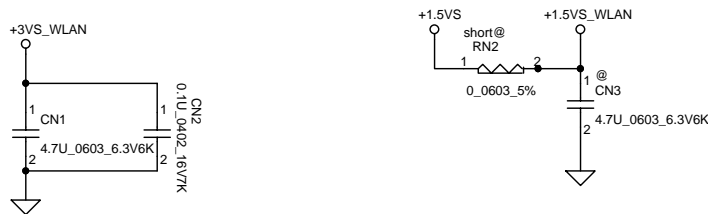
PV# 2013.01.23 Change D\_MIC signals to pin36,37

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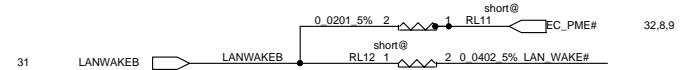
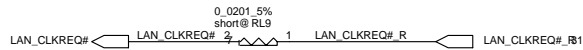


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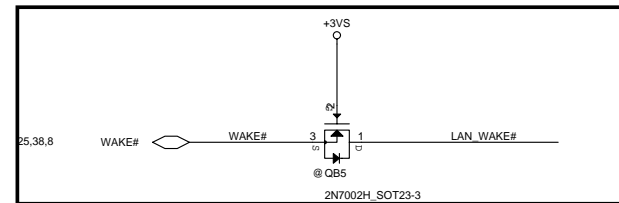
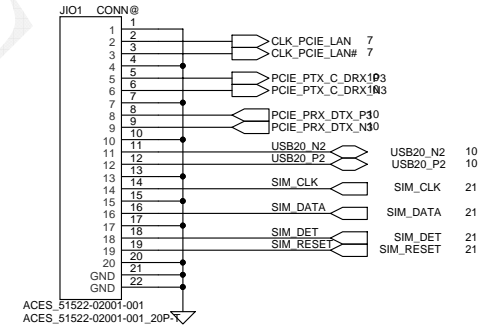




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## 20 Pin FFC

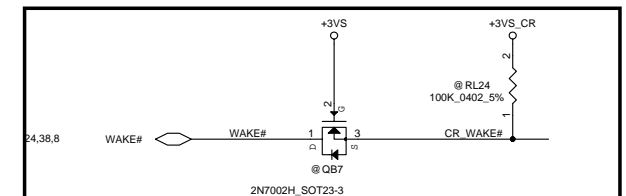


PV# 2013.01.07 Add QB5 abd RL23 to support OBFF

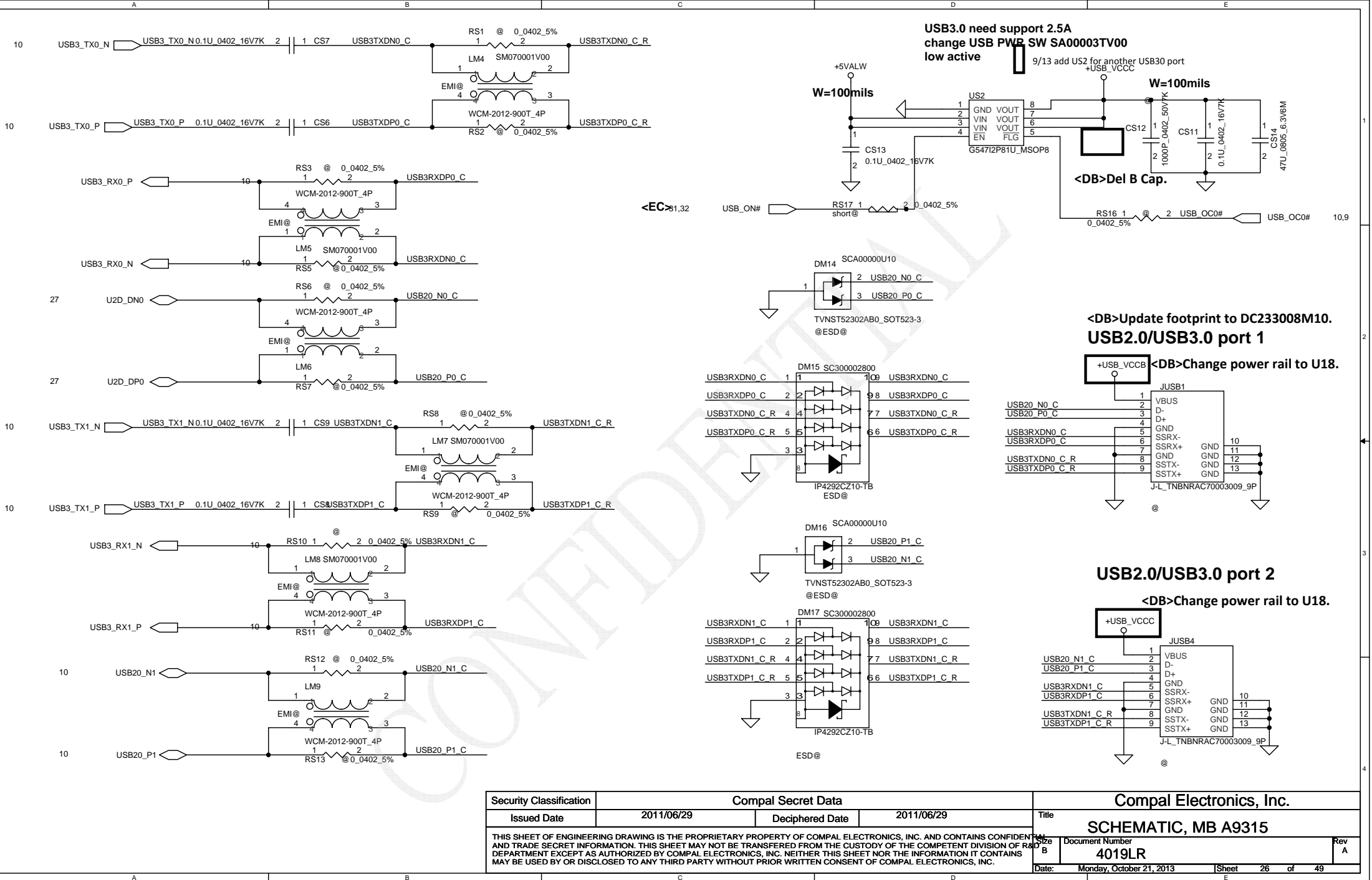
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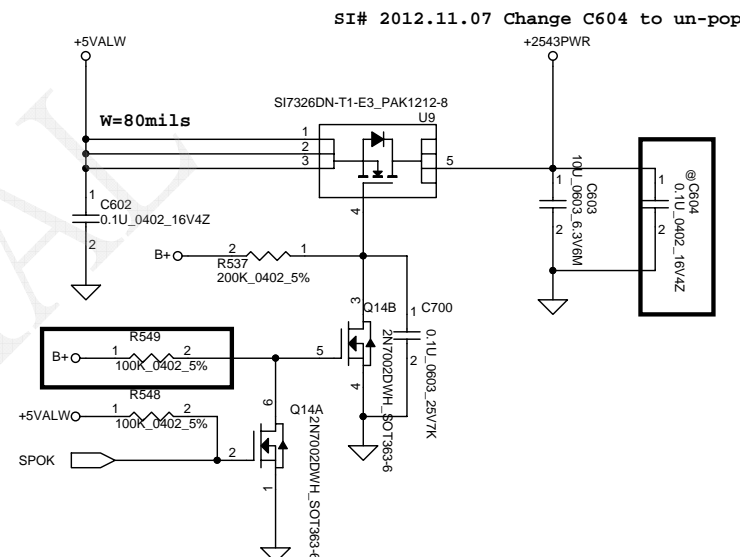
### 9/4 Modify JP10 connector pin defined



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short@ R550 1 2 0 0402 5% USB\_CHARGE\_EN\_R

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+3VS\_AUDIO      short@  
PB2      +DVDD\_IO

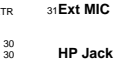
Place AVDD ,PVDD,and DVDD capacitor close to Codec

PLACE CLOSE TO U1 PIN 13

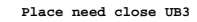
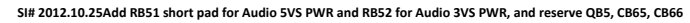
31

PLACE CLOSE TO U1 PIN 14	②	Sense_B to AVDD by 10Kohm resistor
--------------------------	---	------------------------------------

If Sense\_B is un-used, then pull high Sense\_B to AVDD by 10Kohm resistor



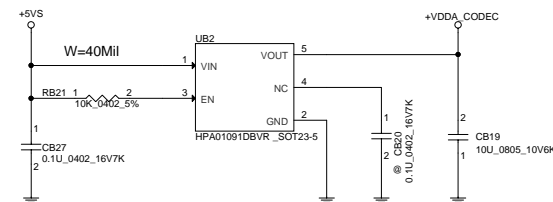
Internal SPKR



### Audio power

***SB Beep***

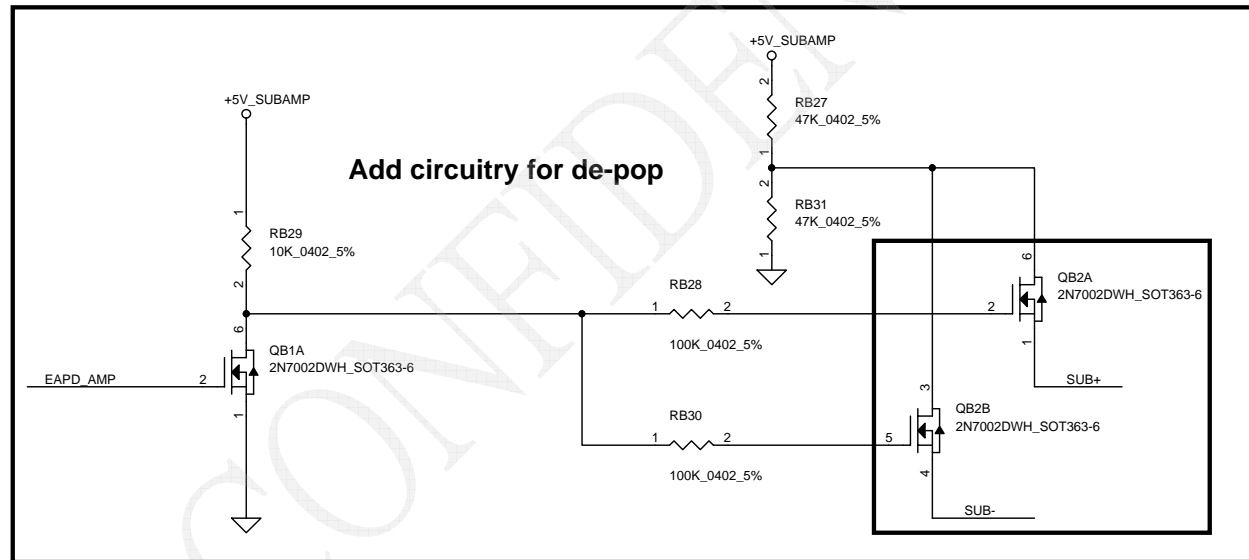
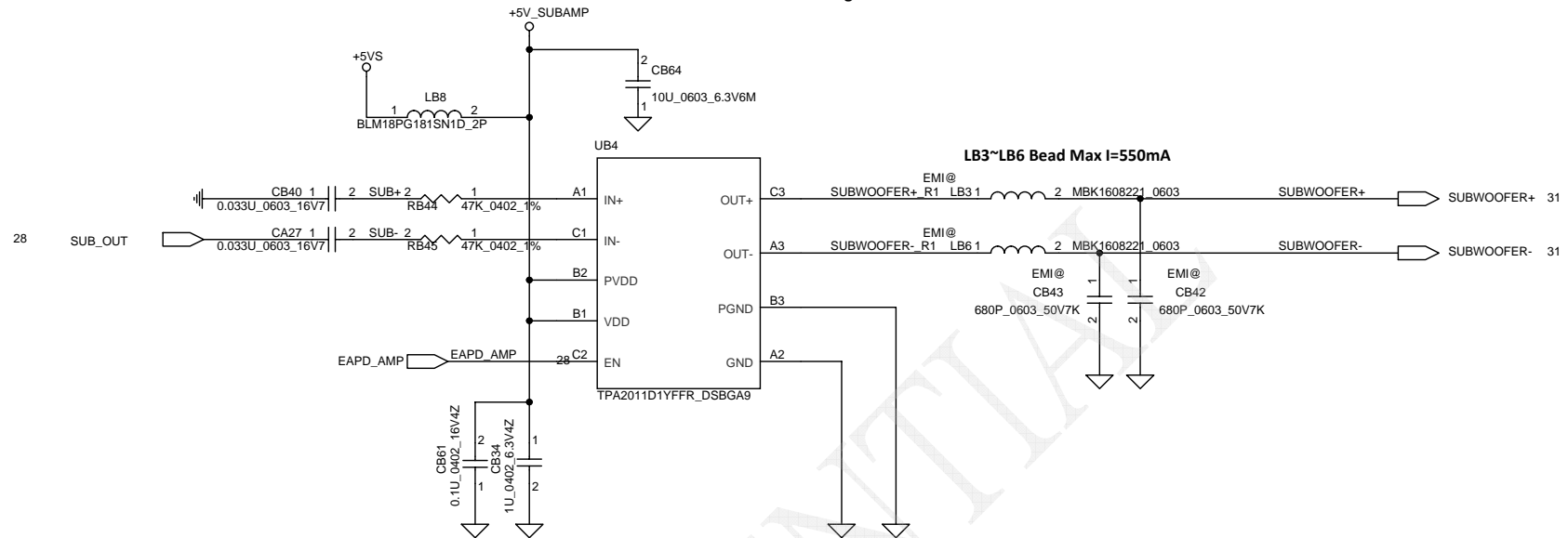
EMI@	CB29	1	2	0.1U	0402	25V6
@EMI@	CB28	1	2	0.1U	0402	25V6
EMI@	CB25	1	2	0.1U	0402	25V6
@EMI@	CB22	1	2	0.1U	0402	25V6
EMI@	CB21	1	2	0.1U	0402	25V6
short@	RB17	1	2	0.0805	5%	



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# Subwoofer AMP TPA2011 = HPA01086YFFR

DB> TPA2012 Change to TPA2011

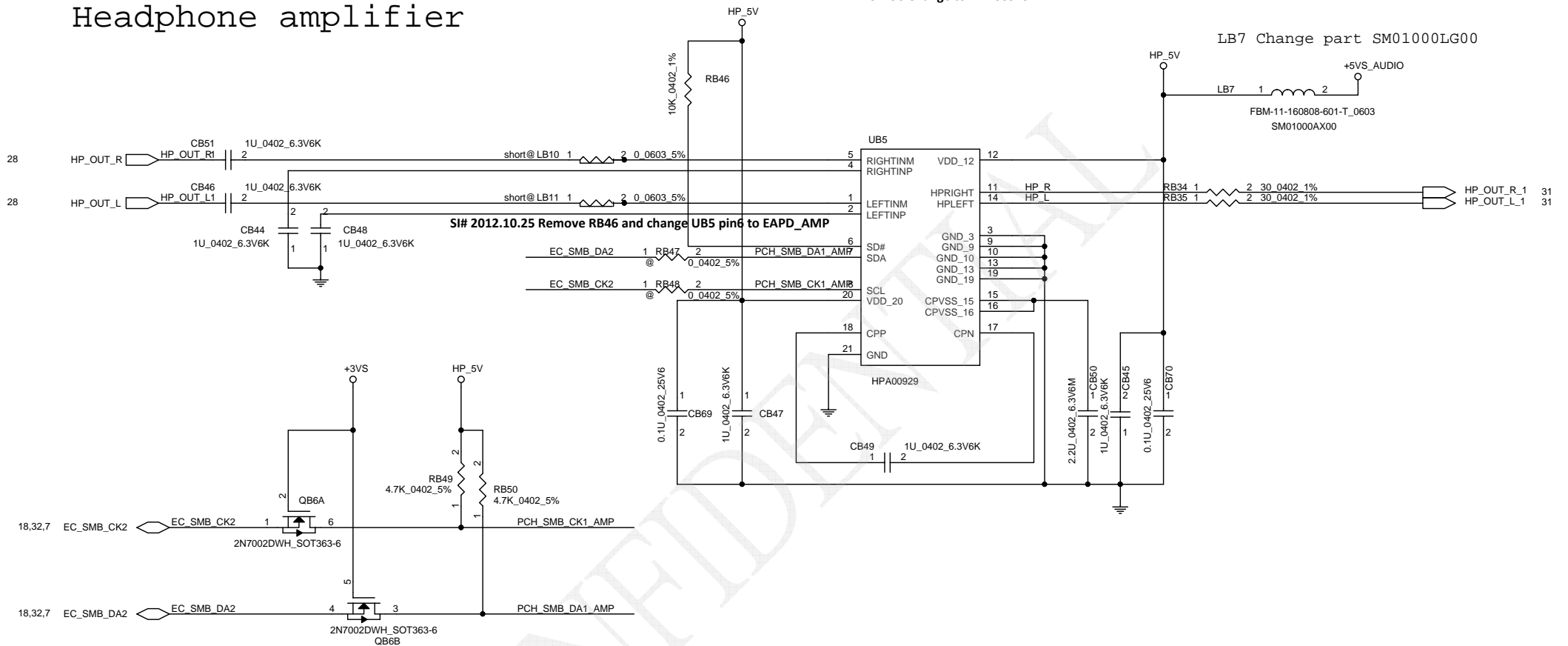


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# Headphone AMP TPA6130A2 = HPA00929

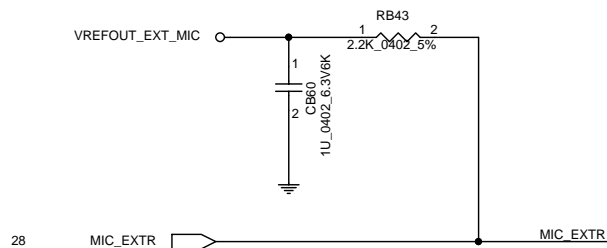
DB> HPA01196 Change to HPA00929

## Headphone amplifier



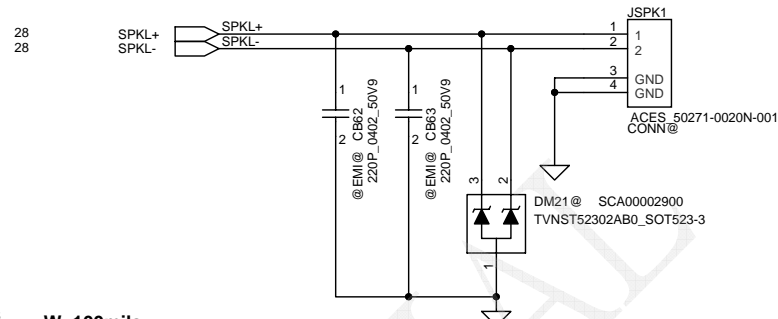
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## Ext. Mic

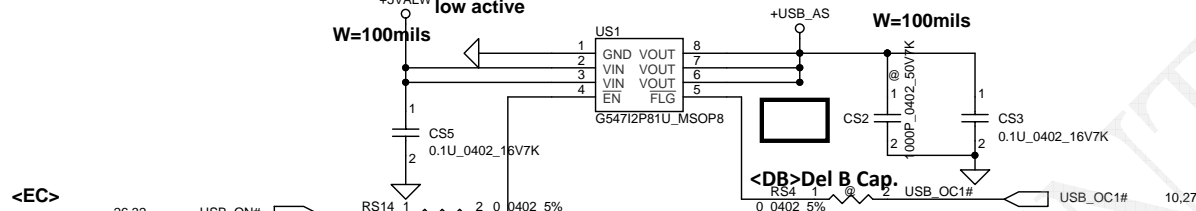


## Front Speaker Connector 1

## SPK conn

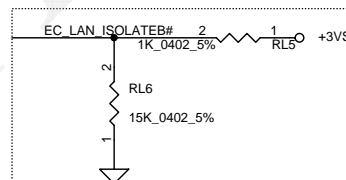
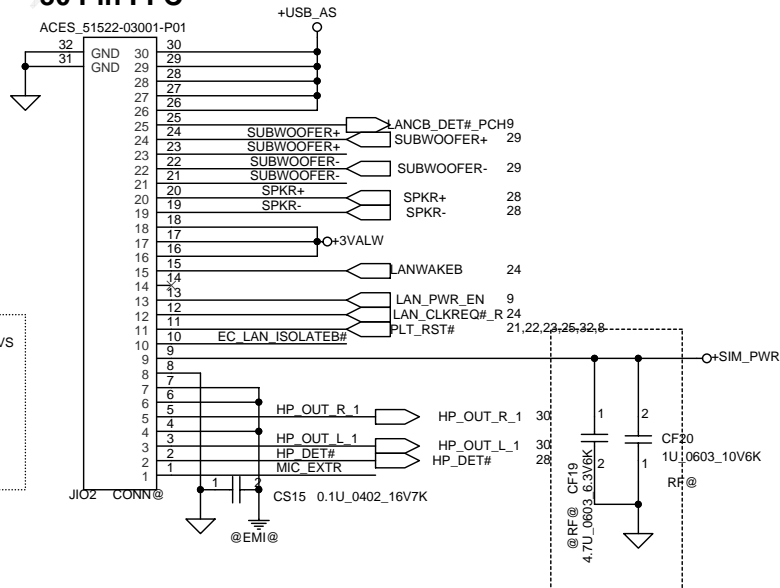


USB3.0 need support 2.5A  
change USB PWR SW SA00003TV00  
low active



<DB>Change power rail to US1.

## 30 Pin FFC



10/30 RF add, near JIO1 connector.

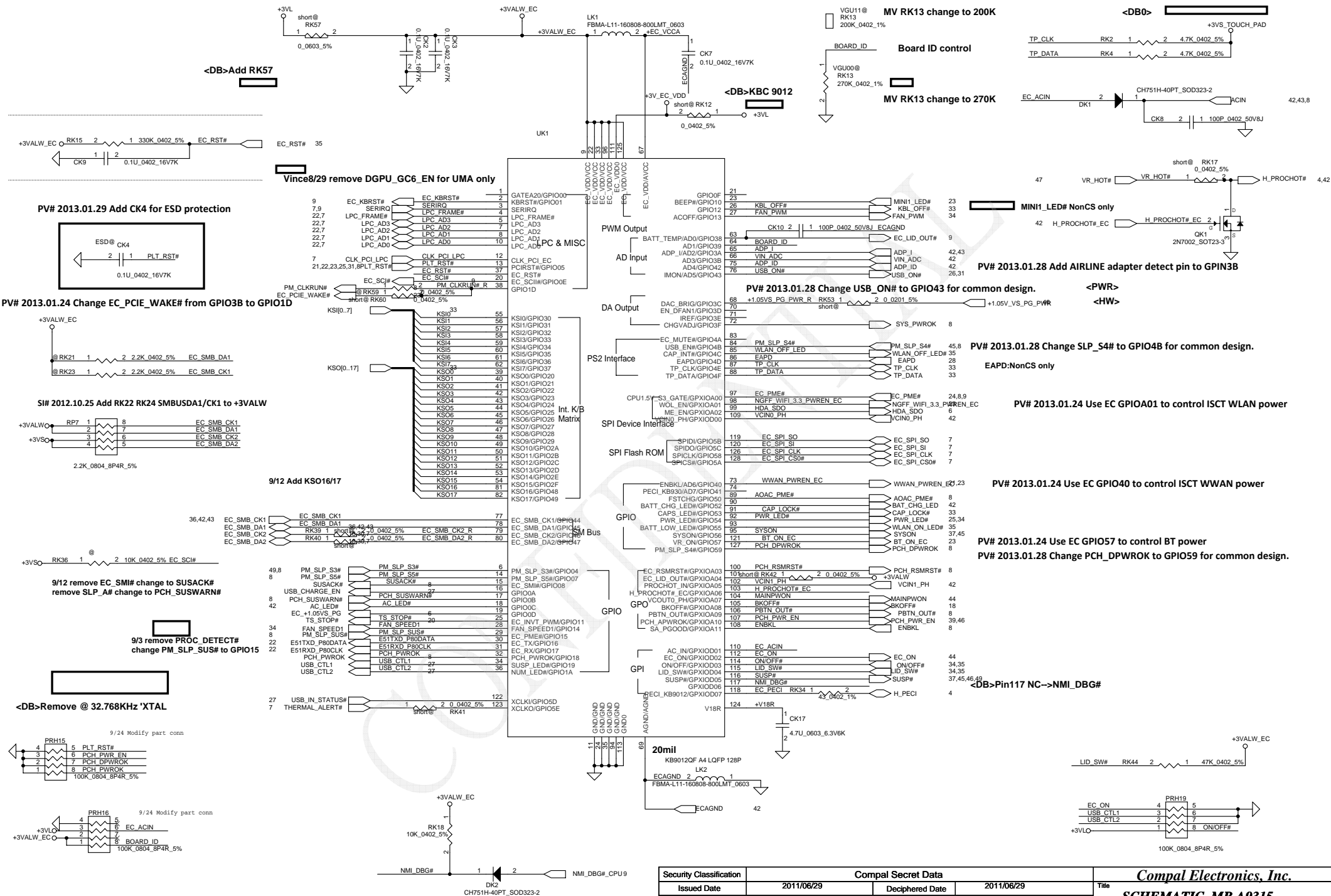
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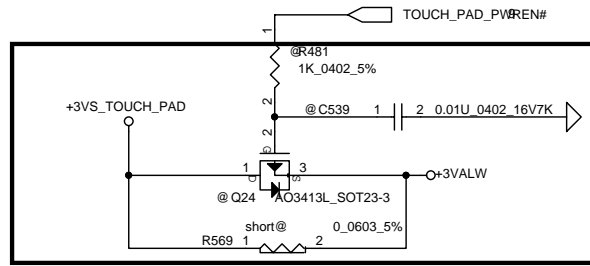
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4019LR

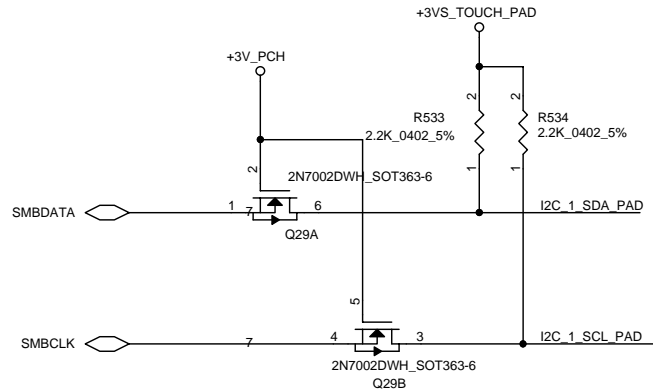


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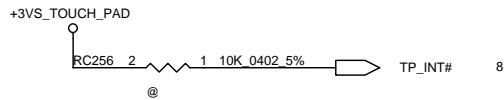




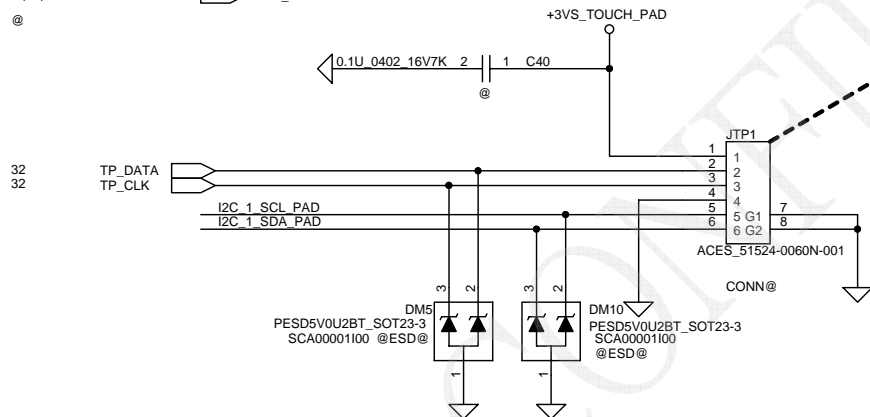
SI# 2012.10.25 Add R569 short pad for Touch PAD PWR, and reserve Q24, R569, R481



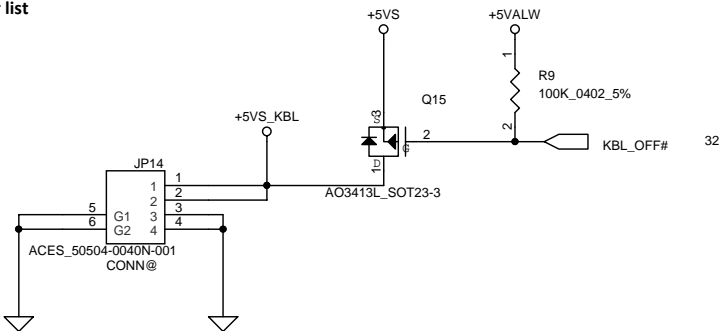
Touch pad conn



PV# 2012.01.08 Change TP connector to 6 pin and pin define

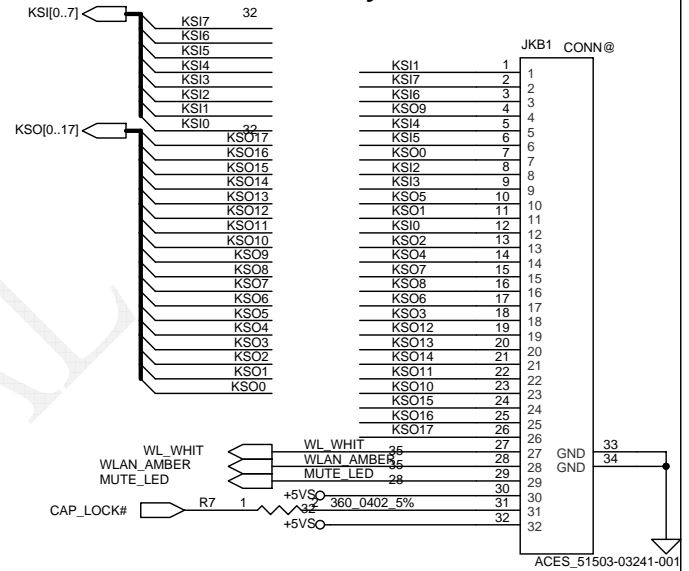


Waiting for connector list

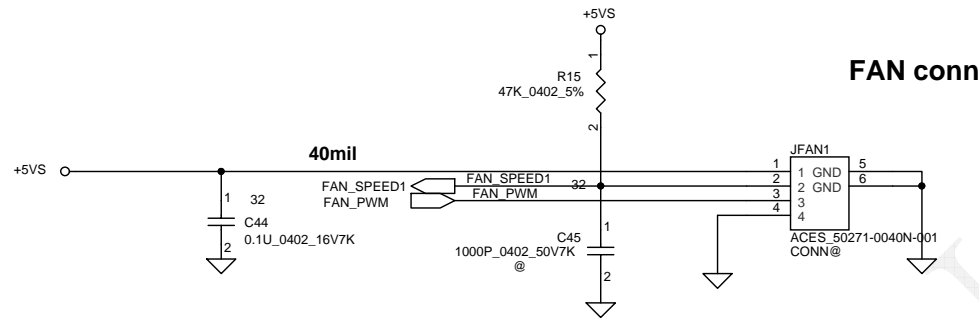


Keyboard backlight Conn

Keyboard conn

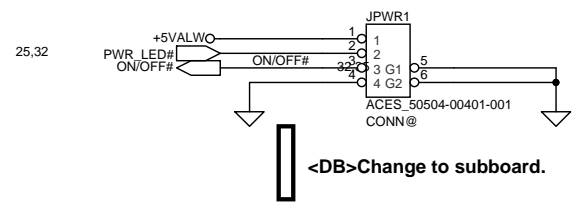


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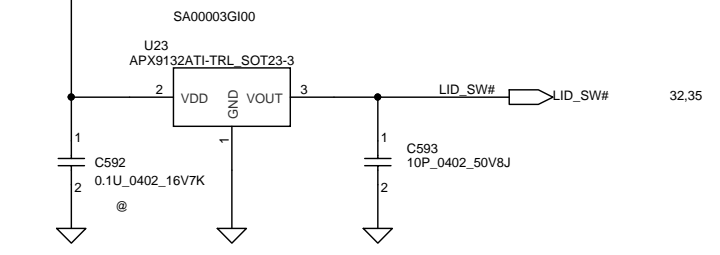
FAN conn

Power Button Connector



Lid Switch (Hall Effect Sensor)

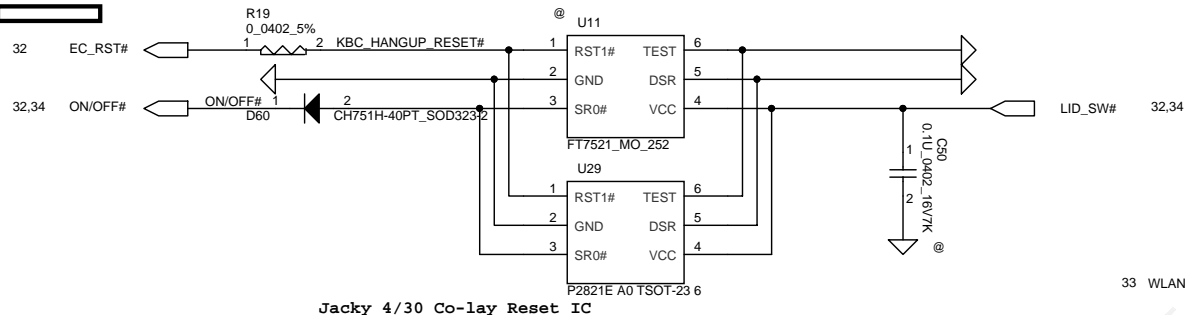
PV# 2013.01.08 Change LID switch power rail to +3VALW\_EC



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<DB> RST1# connect to EN\_3V\_5V

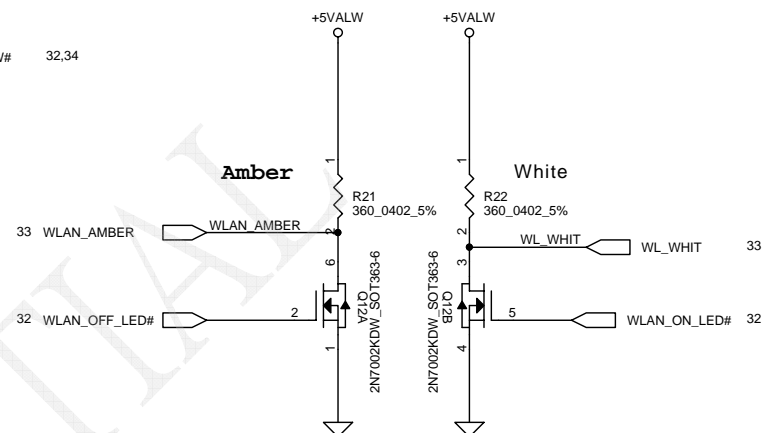
## Reset IC



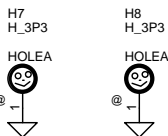
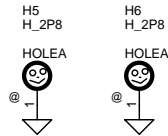
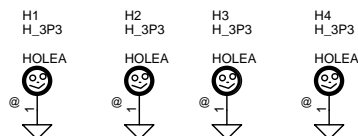
Jacky 4/30 Co-lay Reset IC

Amber

White

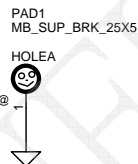
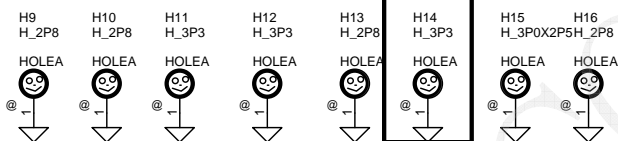


CPU

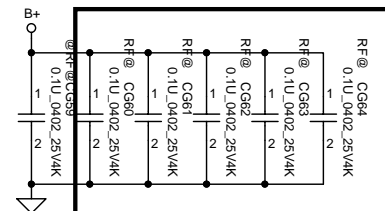
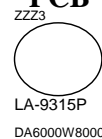


Card reader

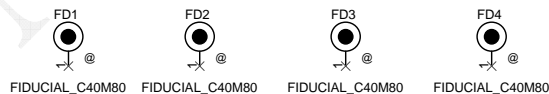
SI# 2012.10.31 Add H14 for WLAN stand off



PCB

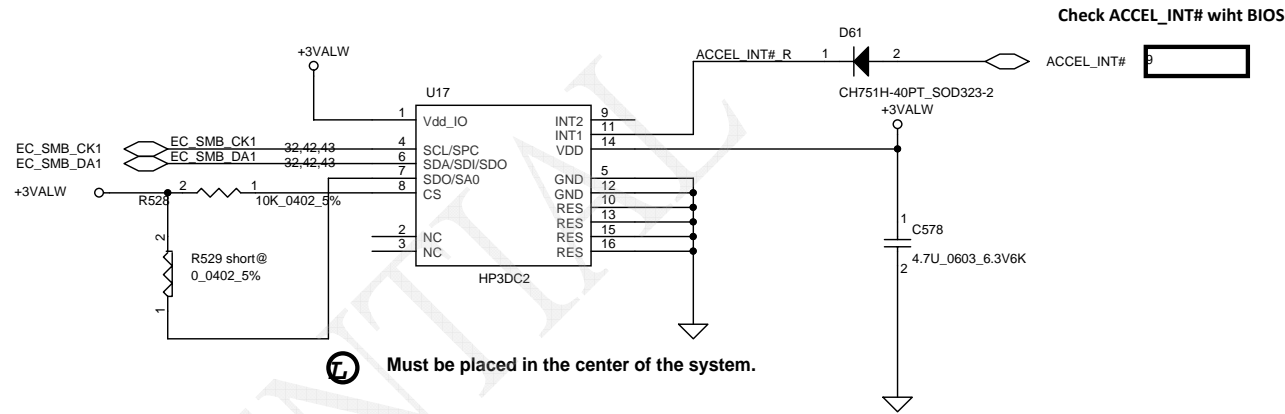


PV# 2013.01.30 Add CG60~CG64 for RF.

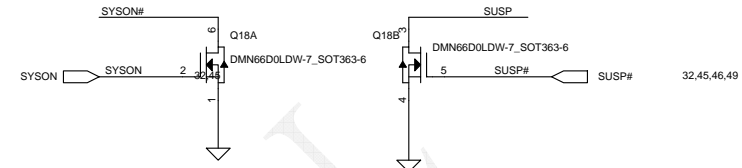


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ACCELEROMETER

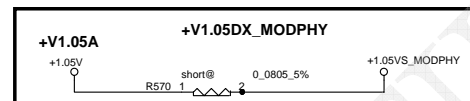
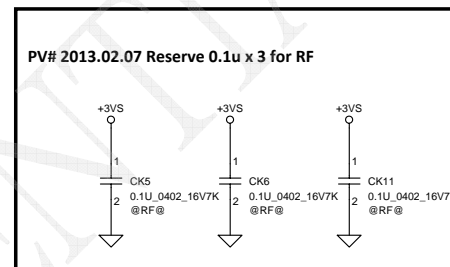


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**J1 need to short**

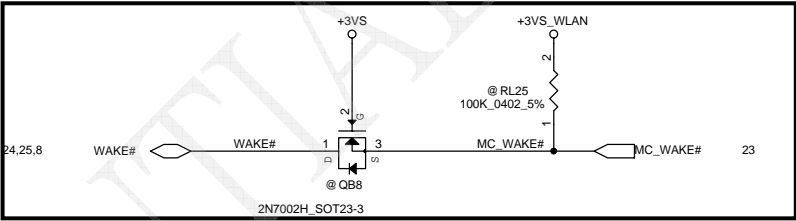
Diagram illustrating a short circuit across J1. The circuit shows two +1.05V sources connected to pins 1 and 2 of J1. The components are labeled J1, JUMP\_43X79, and a resistor symbol.



AO4430L  
VGS Max=+/- 20V  
VGS(Th) max=2.5V  
Rds Max=5.5m @VGS=10V  
Rds Max=7.5m @VGS=4.5V

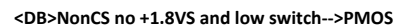
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NGFF and WLAN



PV# 2013.01.23 Add QB8 abd RL25 to support OBFF

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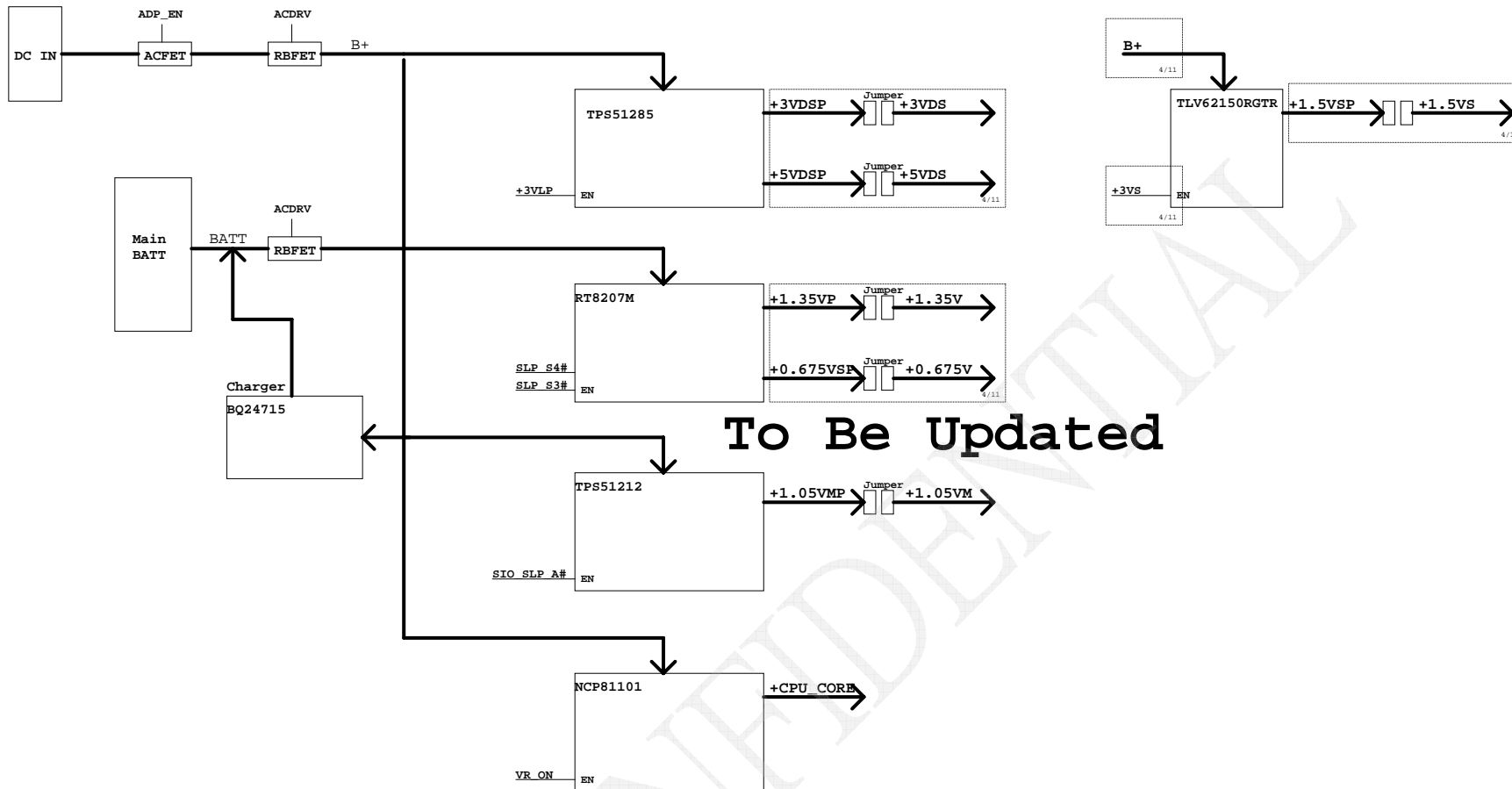
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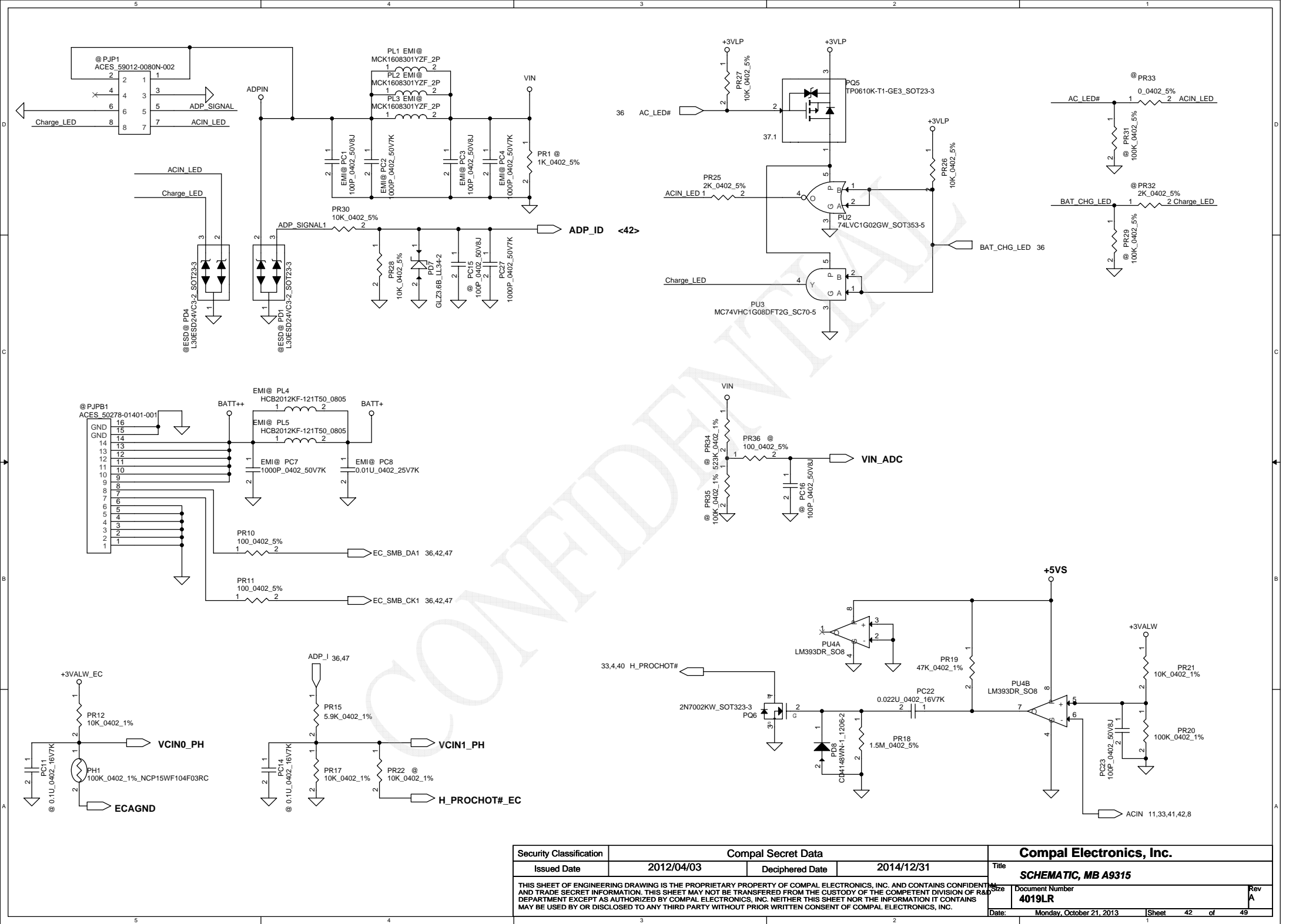
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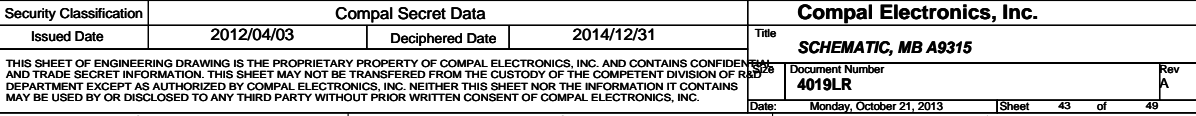
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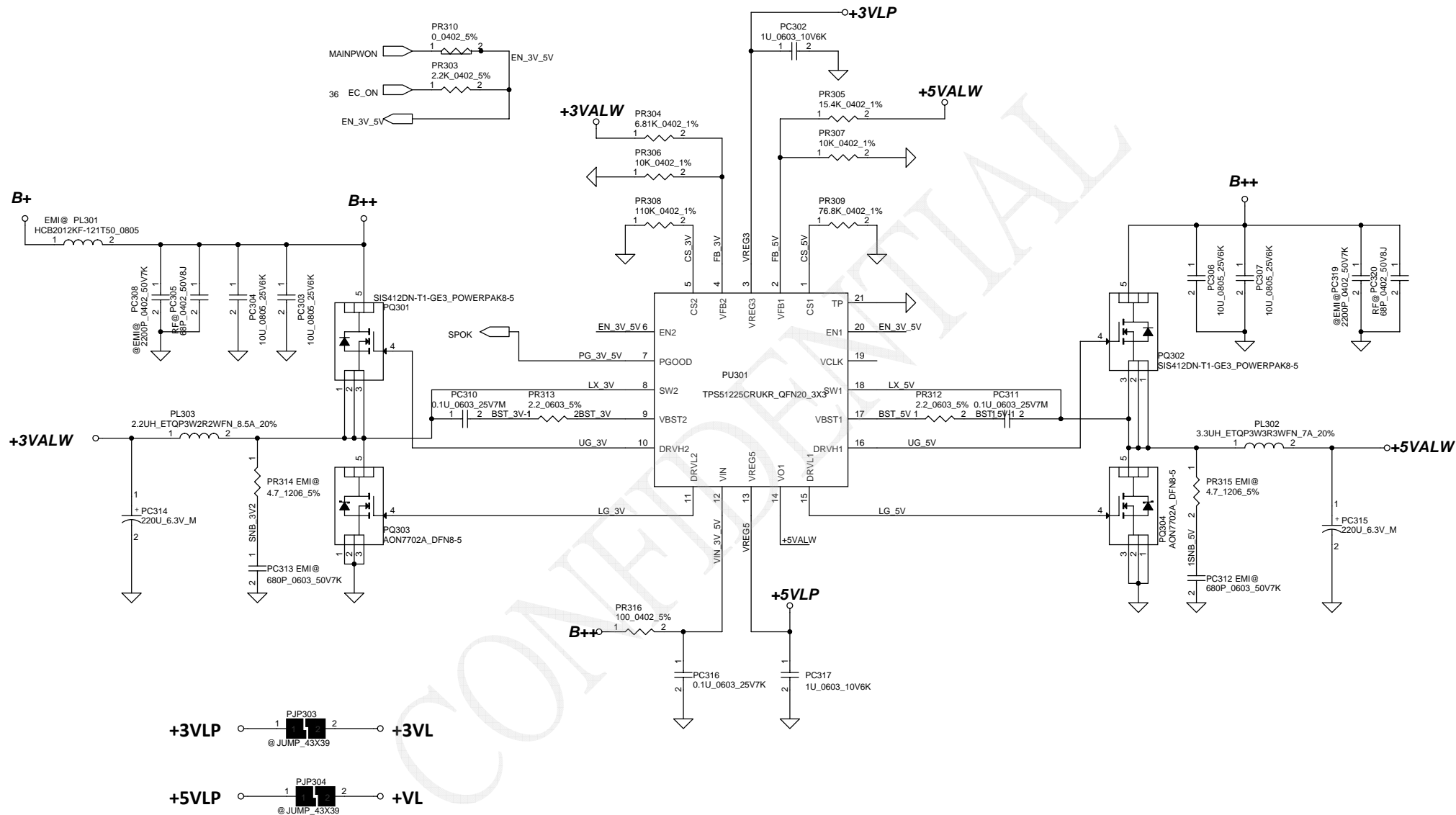




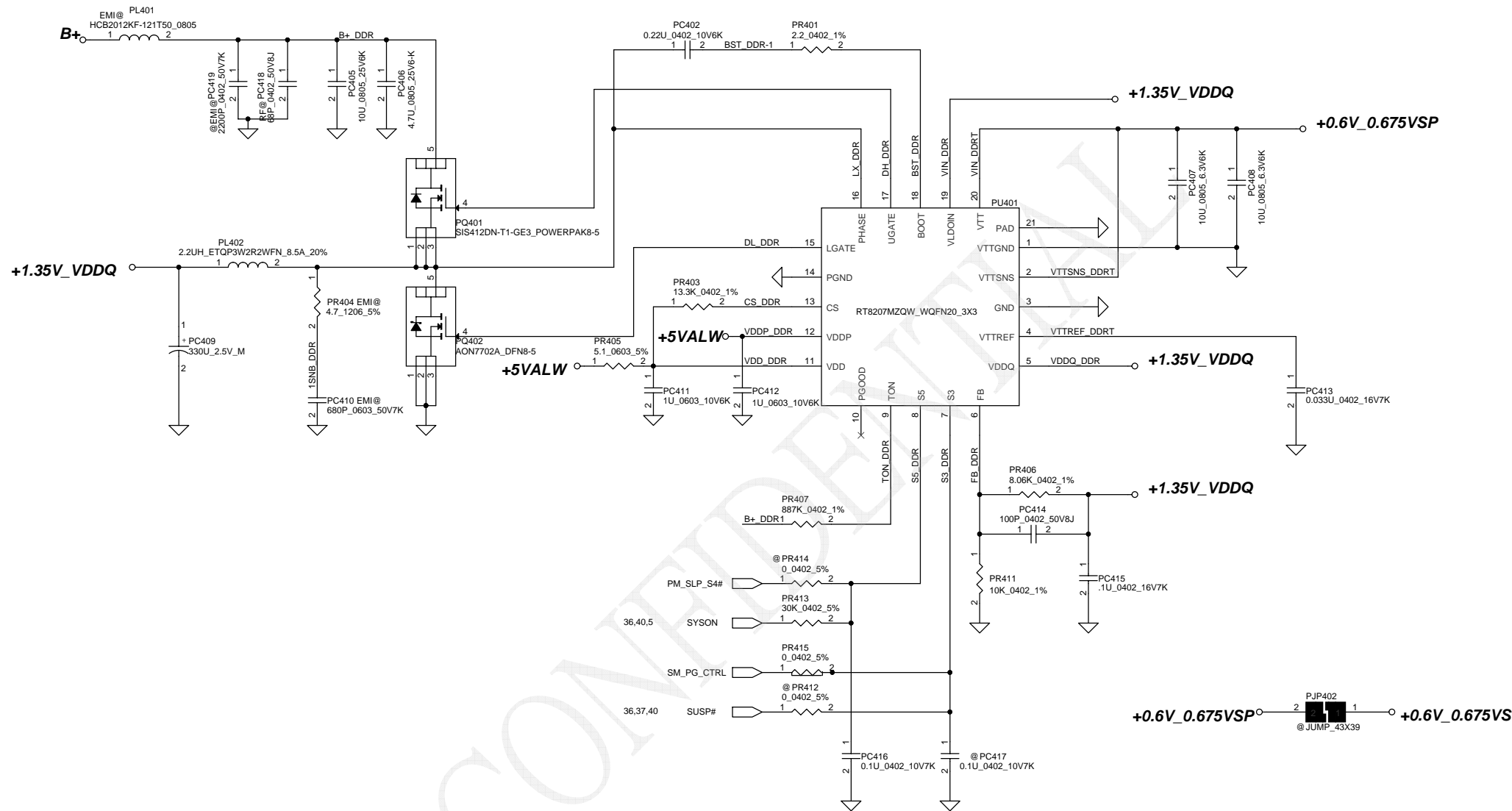
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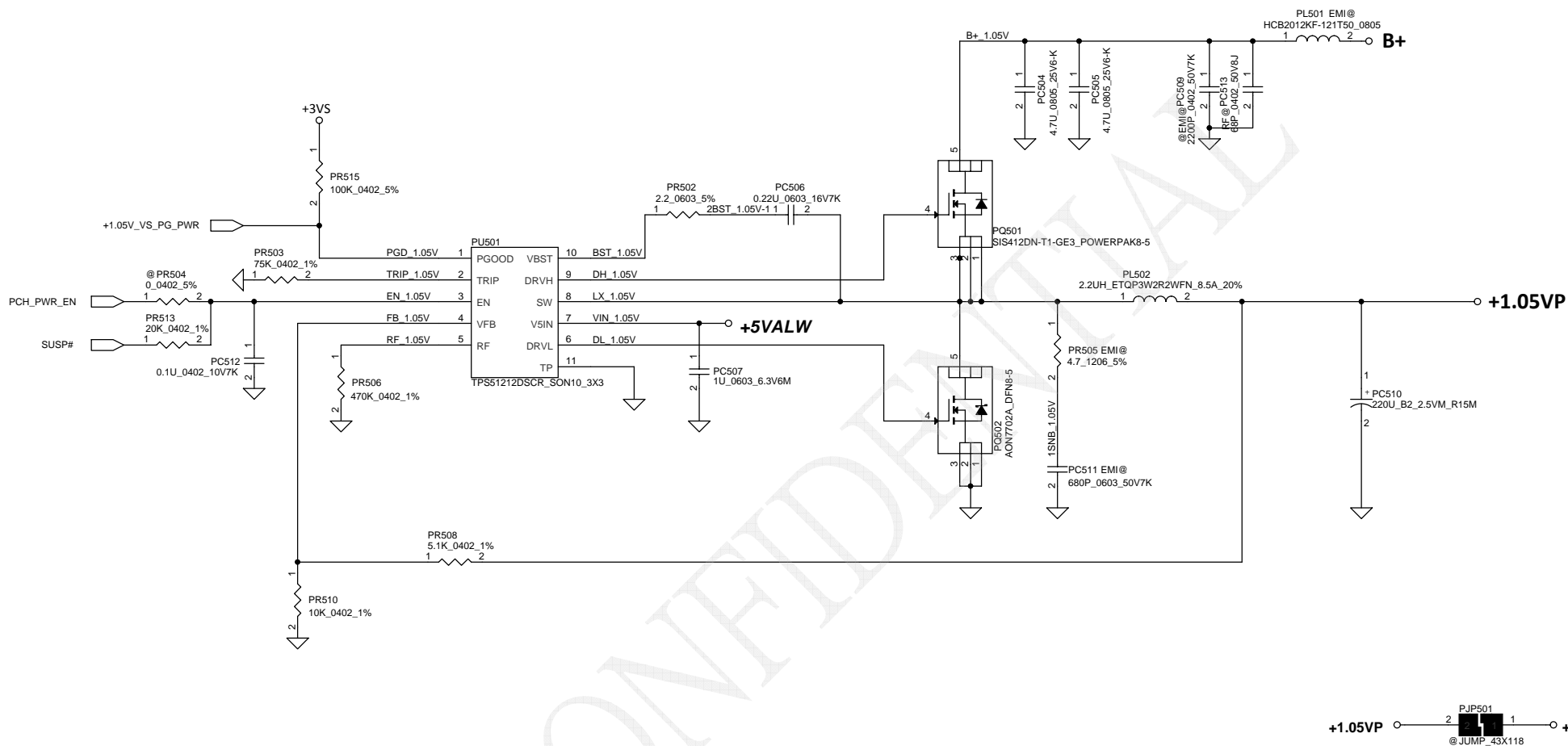




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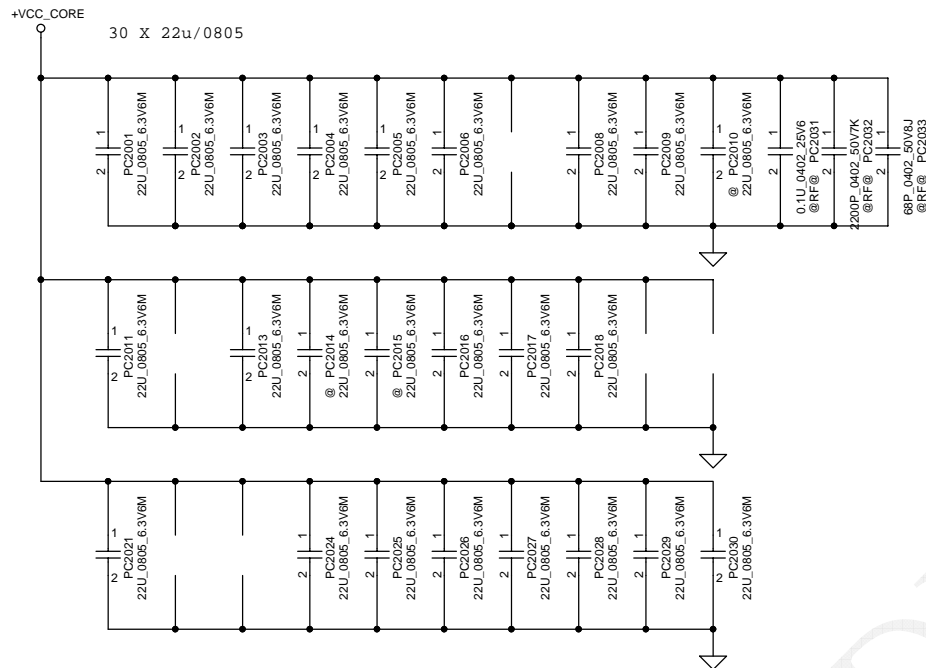


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